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Wideband Phase Shifter Program
Final Report

31 August 1994

Contract N00014-92-C-2211
CDRL No. A002

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Naval Research Laboratory
4555 Overlook Avenue, SW
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An 18-month program was performed to develop a wide band 6-bit phase shifter for phased-array radar modules. A new GaAs control-element FET (CFET) was explored on this program to replace the conventional MESFET. New circuit concepts and topologies were investigated and demonstrated to exploit this new control element. Discrete CFETs and monolithic phase shift bits employing CFETs were demonstrated. CFETs with figures of merit exceeding 400 GHZ were demonstrated. Improvement in device figure of merit would decrease MMIC component insertion loss and increase microwave module performance.

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INTRODUCTION

1.1 PROGRAM RATIONALE

To provide low insertion loss for wideband microwave monolithic control circuits, such as switches, phase shifters and attenuators, a new gallium arsenide (GaAs) device has been demonstrated. Known as a CFET, for Control Field Effect Transistor, this device eliminates the need for a conventional submicron gate MESFET or PIN diode switching device typically used in monolithic microwave integrated circuits (MMICs). Device capacitance is smaller than a conventional MESFET, resulting in a higher figure of merit (FOM). This FOM translates into broader bandwidth potential for MMIC components. First demonstrated as part of a Texas Instruments (TI) Independent Research and Development (IR&D) effort, the CFET was introduced into this NRL-sponsored program as a device offering significant performance advantage over the MESFET (because of lower loss) and the PIN diode (because of lower dc power consumption) in control circuit applications. In wideband transmit/receive (T/R) modules, this performance enhancement would improve receiver noise figure and third-order intercept (TOI), resulting in greater dynamic range. Depending upon the module architecture, the combined lower rf insertion loss of several CFET control MMICs could potentially eliminate a transmit or receive gain stage.

Although excellent device performance was demonstrated prior to this program, attempts to improve the device repeatability for eventual insertion into T/R modules and systems were not totally successful. This report summarizes the progress made and the lessons learned during the course of this effort.

The objective of this program was to develop a 6-bit phase shifter for wideband transmit/receive (T/R) modules using this new control-FET device. Specific performance goals for the wideband phase shifter are summarized in Table 1-1. The program was conducted in two phases. The first phase dealt with optimization of the CFET material structure and fabrication steps. The second phase involved design and demonstration of monolithic phase shift bits using this device.

TABLE 1-1. WIDEBAND 6-BIT PHASE SHIFTER GOALS

Parameter	Goal
Frequency (GHz)	6 to 18
Insertion loss (dB)	8.5
RMS phase error (degrees)	10
Switching time (nS)	50
Control voltage (V)	-10, +3
Control current (μm)	10/bit
Maximum chip size (inch)	0.080 × 0.150
Input/output VSWR	<2.0:1
TOI at input (dBm)	>20

TEXAS INSTRUMENTS

27 September 1994

In Reply Refer to:
232-234-3871

Naval Research Laboratory
Code 6851
4555 Overlook Avenue, SW
Washington, D.C. 20375-5320

ATTENTION: Harvey Newman

SUBJECT: Contract No. N00014-92-C-2211

ENCLOSURE: (1) Final Report, Sequence No. A002
(2) DD250

Sir:

Enclosures (1) and (2) are hereby submitted in accordance with the requirements of the subject contract. If you require additional technical information in support of this submittal, please contact the undersigned at (214) 995-6314. If you have questions concerning contractual matters, please contact Ms. Christine Guyton, Contracts Administrator, at (214) 995-6711.

Sincerely,

Randall E. Lehmann

Randall E. Lehmann
Program Manager
MMIC Technology

REL:jd

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Sincerely,

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Program Manager
MMIC Technology

REL:jd

SECTION 2
CFET DEVICE

2.1 BACKGROUND OF INVENTION

In most microwave radars, signal processing is required to achieve high performance in today's hostile and unpredictable environments. This signal processing requires control of the signal, both transmitted and received, in amplitude and phase. Illustrated in the block diagrams of Figure 2-1, these systems liberally use control elements for functions such as switches, attenuators, phase shifters, and limiters. This section will examine the tradeoff of performance of several monolithic GaAs elements for use as control elements and introduce the back-gate FET (BGFET).

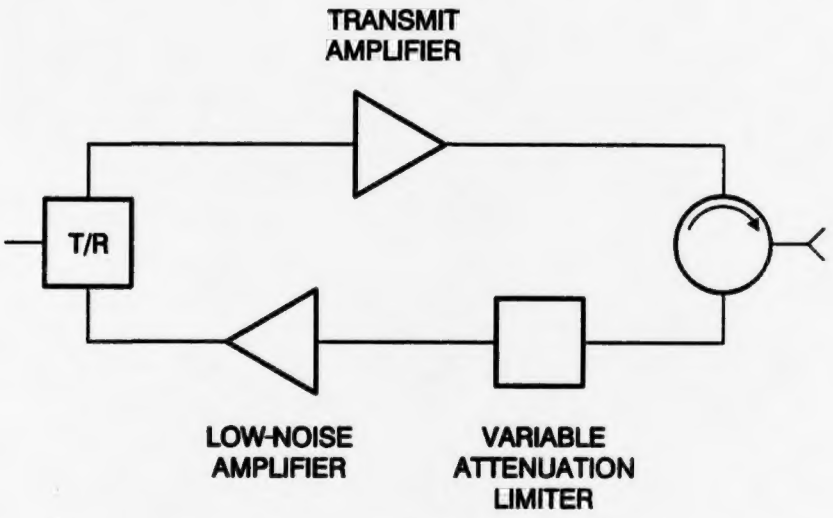

Figure 2-1. Block Diagram of Radar Module

Parasitic components of monolithic elements (i.e., source resistance, stray capacitance) will reduce their performance as control elements. However, since many of these parasitic components are design and/or process related they will not be included in this tradeoff study. Only the intrinsic device parameters of the control elements will be evaluated. This summary is intended to evaluate their ultimate performances as control elements.

2.1.1 Figure of Merit

In any control application the two major design parameters are the on-impedance (R_{on}) and the off-impedance (R_{off}). In a monolithic element the off-impedance is the reactive impedance of the terminal-to-terminal capacitance (C_{off}). Therefore a figure of merit (FOM) expressed as a frequency is used to evaluate various control elements.

$$Figure\ of\ Merit\ (FOM) = \frac{1}{2\pi R_{on} C_{off}}$$

Another parameter, ratio of merit, was developed as part of the NRL wideband switch contract. This ratio of merit expresses what value R_{on} or C_{off} may not exceed to meet the circuit performance requirements. For example, the device may be scaled in size to reduce R_{on} but at the expense of C_{off}. Obviously a limit exists where the device cannot be scaled beyond where C_{off} will limit the circuit performance. The figure of merit is a better device evaluation parameter. The ratio of merit is more useful as a circuit design tool.

2.1.2 Control Devices

2.1.2.1 FET

Figure 2-2 is a photograph of a 300-μm gate width FET current-voltage (IV) curve at zero drain-source voltage. Figure 2-3 illustrates a cross section of an FET. The on-resistance at zero drain-source voltage is the resistance directly under the gate and can be expressed by the standard resistance formula.

$$R_{on} = \rho \frac{L}{A}$$

R_{on} for the FET, when the gate is forward biased to the point when the depletion layer under the gate is reduced to zero, is

$$R_{on} = \frac{1}{q\mu N_d} \frac{L_g}{W_g T}$$

where

μ = electron mobility
N_d = doping concentration
W_g = gate width

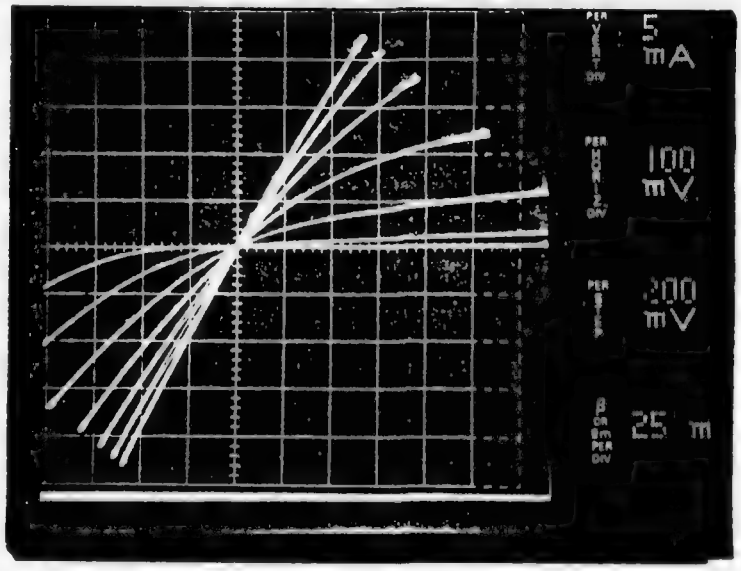

Figure 2-2. FET I/V Curves

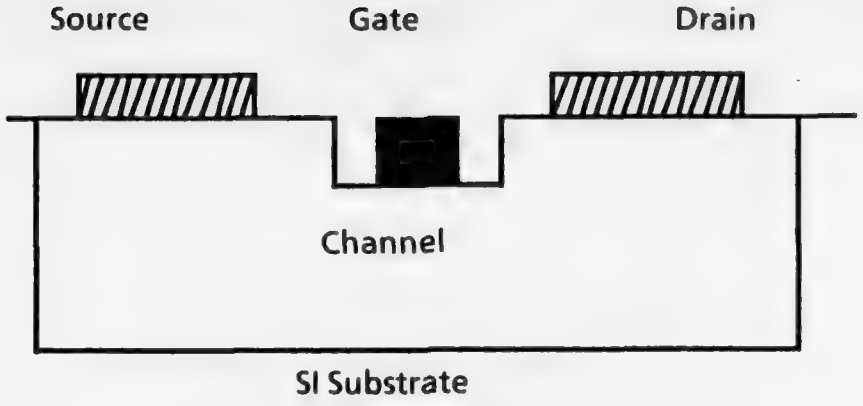

Figure 2-3. FET Cross Section

L_g = gate length
T = layer thickness.

This equation illustrates the effect of scaling on R_{on} with changes in gate width. This equation also encompasses high electron mobility transistors (HEMTs) by the effect of higher mobility. To reduce R_{on} the doping density and thickness should be increased. The thickness and doping is limited by the requirement that the breakdown voltage exceeds the voltage required to pinch off the channel. Figure 2-4 shows the relationship between doping, thickness, and

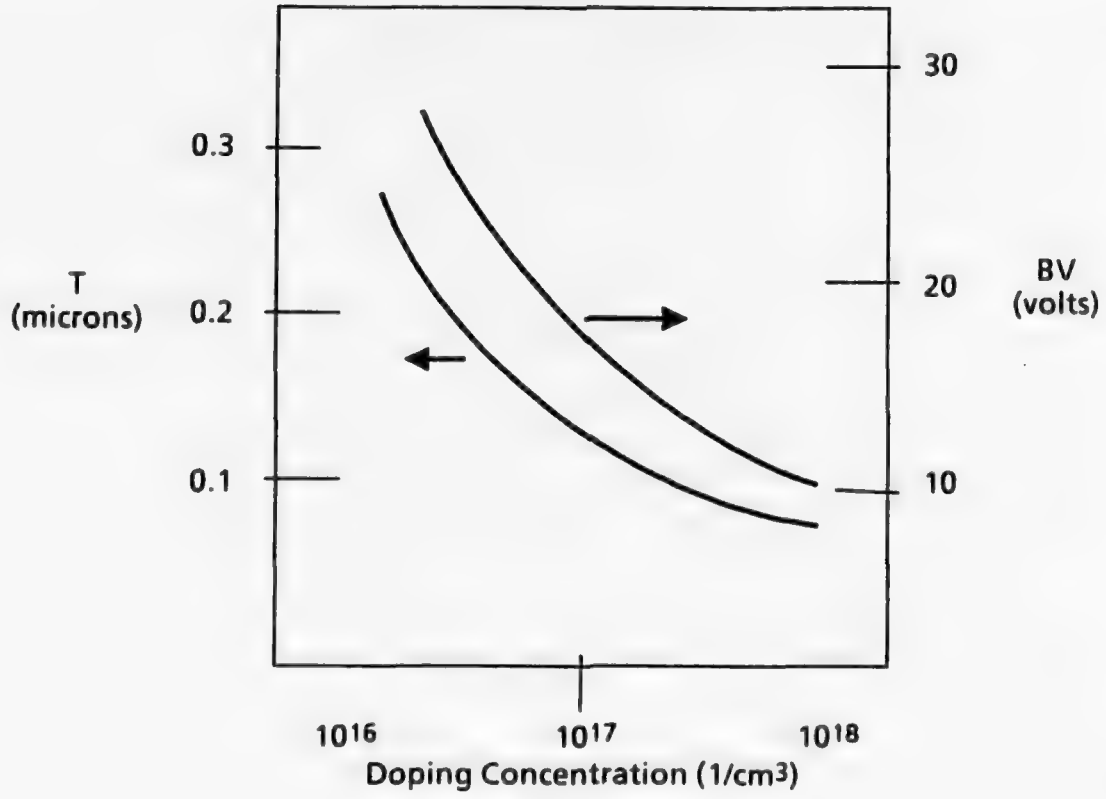

Figure 2-4. T, BV Versus N_d

breakdown voltage for GaAs using 5 volts as the pinch-off voltage. System requirements, such as voltage supply availability, usually determine the maximum pinch-off voltage allowed.

Referring to Figure 2-3, the off-capacitance can be expressed as the capacitance under the gate at pinch-off as

$$C_{off} = \frac{\varepsilon_s L_g W_g}{4T}$$

The 4 comes from the gate capacitance divided in two and then summed in series electrically. By combining the equations for R_{on} and C_{off}, the figure of merit can be computed as

$$FOM = \frac{2q\mu N_d T^2}{\pi \varepsilon_s L_g^2}$$

This shows that the layer thickness and gate length are the major factors in increasing the figure of merit.

By substituting the depletion layer thickness as a function of N_d and applied voltage, the FOM can be expressed as

$$FOM = \frac{4\mu n(V_{bi}+V)}{\pi L_g^2}$$

where

V = maximum pinch-off voltage
V_{bi} = built-in potential (~ 0.6 v).

This equation shows the sensitivity of FOM on gate length and mobility. A HEMT would have a higher figure of merit because of its higher mobility. The applied voltage should be as high as system voltage supplies and power handling permits.

As an example, assume the power handling requirement is 1 watt and the supply voltage is 5 volts. The breakdown voltage must then be in excess of

$$V_{bv} > V_{supply} + 2\,(V_{peak})$$
$$> 25 \text{ volts (for 1 W power handling)}$$

Referring to Figure 2-4, the doping must be less than 1×10^{17} to achieve this breakdown voltage. Series connected FETs can be used to raise the operating voltage level and does not affect the figure of merit.

Figure 2-5 shows the figure of merit for 5-volt supply operation versus gate length. The high FOM compared to measured results indicate that the FET is dominated by parasitic components, mainly source and drain resistance.

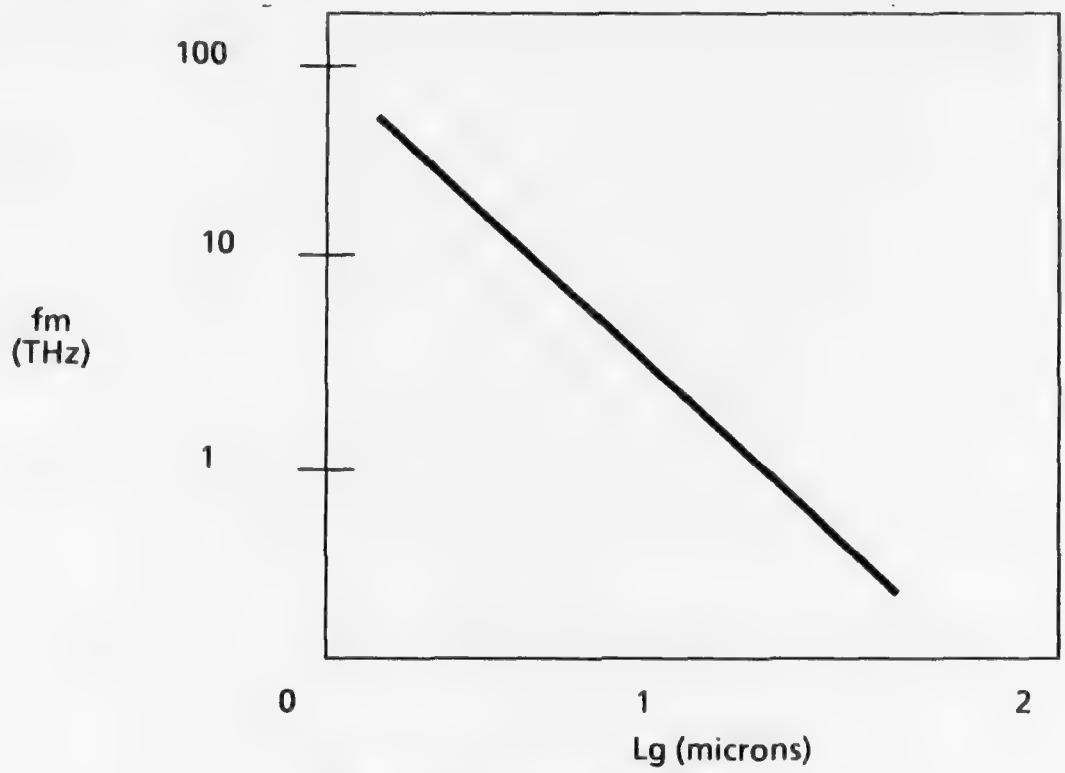

Figure 2-5. Figure of Merit Versus L_g

2.1.2.2 PIN Diode

The on-resistance of a PIN diode can be expressed by

$$R_{on} = \frac{W_i^2}{2\mu IT}$$

where

W_i = intrinsic layer thickness
μ = ambipolar mobility
I = forward current
T = storage time.

Note that the on-resistance is independent of device area.

The off-capacitance can be expressed as

$$C_{off} = \frac{\varepsilon_s A}{W_i}$$

where

A = device area.

Combining these two equations yields the figure of merit,

$$FOM = \frac{\mu I T}{\pi W_i \varepsilon_s A}$$

This equation shows the important parameters to optimize for a PIN diode, and that the FOM is area-dependent for a PIN diode. The W_i should be optimized for breakdown voltage which is

$$V_{bv} = E_m W_i$$

where

E_m = maximum field strength (3×10^5 v/cm for GaAs)

For 1-watt power handling the breakdown voltage should exceed 20 volts or $W_i = 0.7$ μm.

Figure 2-6 shows the figure of merit for a PIN diode versus device area with $W_i = 0.7$ μm and I = 20 mA. This also indicates the PIN is dominated by parasitic components, namely resistance, but has a higher intrinsic FOM than FETs.

2.1.2.3 Heterojunction Bipolar Transistor (HBT)

Figure 2-7 shows the IV curves of an HBT. The HBT does not exhibit similar IV curves at zero collector-emitter voltage as compared to the FET. The HBT must draw current to operate in a low impedance state. The HBT circuit must include dc current paths and from this standpoint it offers no circuit advantage over a PIN diode. Again neglecting parasitic elements, the collector current can be approximated by

$$I_c = MA[e^{\frac{qV_{cb}}{nKT}} - 1]$$

where

A = device area
M = constant of material parameters
V_{cb} = collector-base voltage
n = ideality factor.

Therefore, from the usual diode equations,

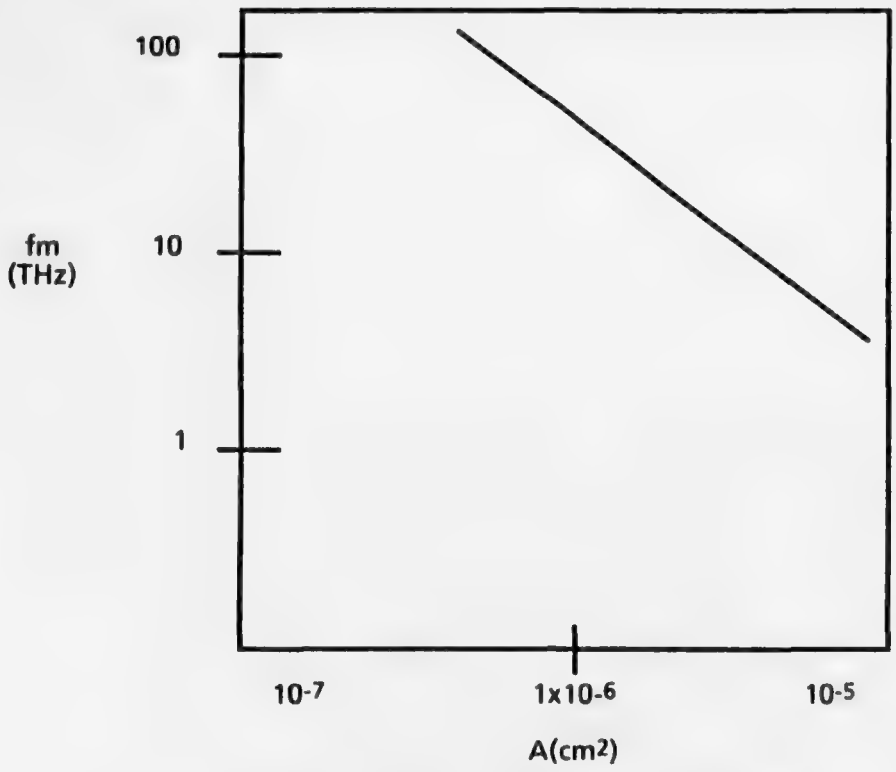

Figure 2-6. Figure of Merit Versus Area for PIN

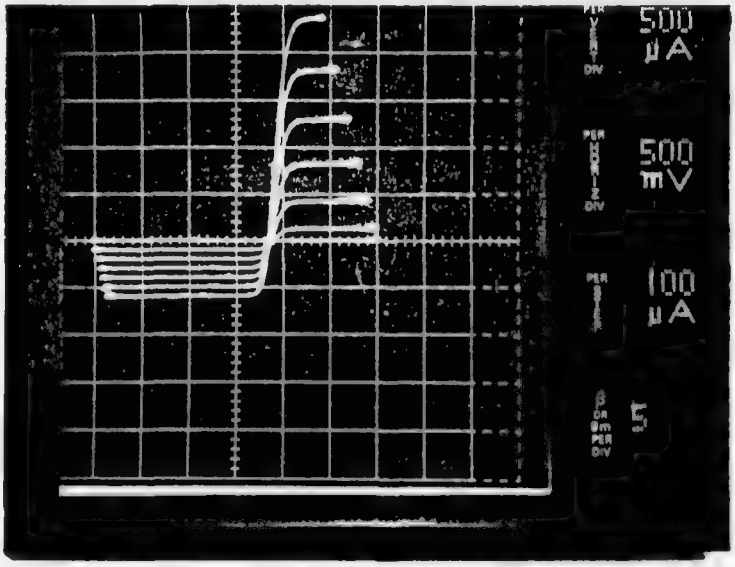

Figure 2-7. HBT I/V Curves

$$R_{on} = \frac{nKT}{qI_c}$$

where

I_c = collector current.

The off-capacitance can be expressed similarly to the PIN diode since the collector region and doping can be chosen to be fully depleted at zero volts and the width chosen for breakdown voltage. C_{off} can be computed as

$$C_{off} = \frac{\varepsilon_s A}{W_c}$$

where

W_c = width of collector layer.

The figure of merit is expressed as

$$FOM = \frac{qW_c I_c}{2\pi nKT\varepsilon_s A}$$

This expression indicates that the figure of merit for a HBT can be scaled with device area, similar to a PIN diode. Figure 2-8 shows the figure of merit versus device area for a HBT with W_c = 0.7 μm and I_c = 20 mA.

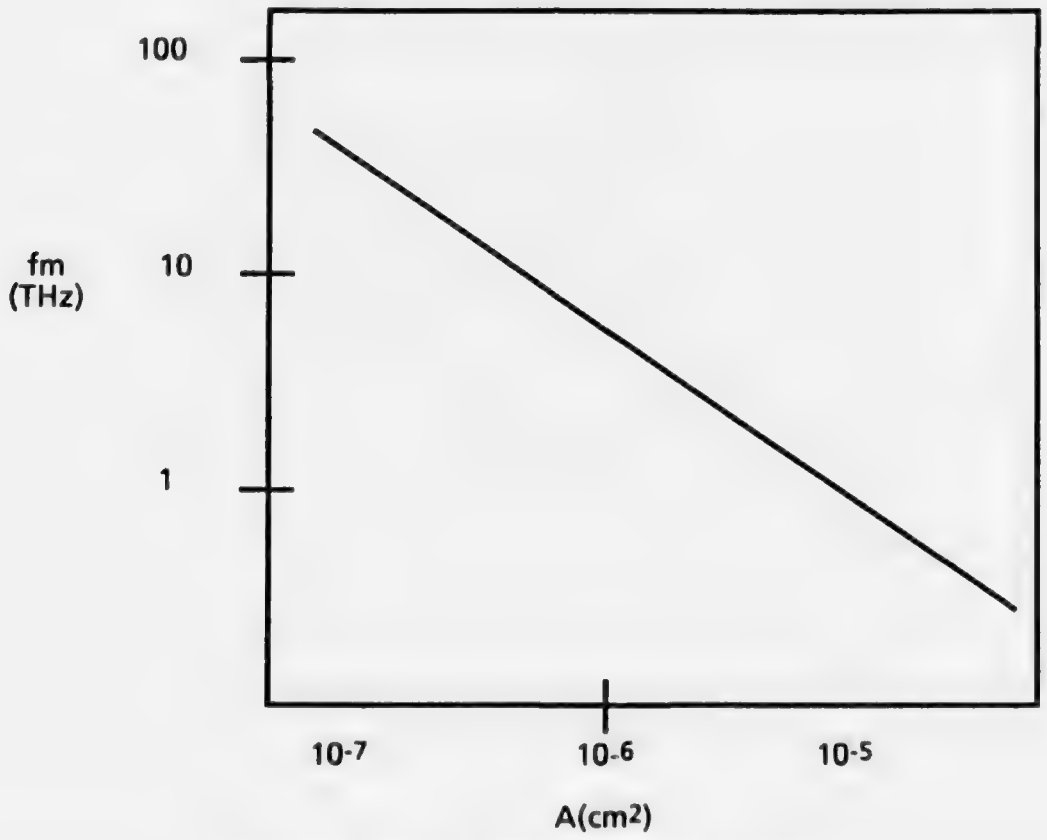

Figure 2-8. Figure of Merit Versus Area for HBT

2.1.2.4 Control FET

Referring to Figure 2-3 of the cross section of an FET, the major component of C_{off} is the capacitance of the gate. If the gate could be remotely placed but still control the resistance of the channel, then this capacitance could be reduced. In addition, the source-drain spacing could be reduced. Such a structure could be fabricated as in Figure 2-9. The source-drain contacts would be replaced by a Si_3N_4 layer, thus providing dc isolation of the input and output transmission lines. This capacitance could serve as a blocking capacitor. The control of this channel would be from the back-side gate. When the back-gate is biased positive with respect to the channel the channel is conductive. The signal is capacitively coupled from one transmission line to the other through the channel. When the back-gate is biased negative relative to the channel, the channel is fully depleted and control element is off. The C_{off} would be the capacitance between the input and output transmission lines. This structure has the advantage that it does not require ohmic contacts or a gate in the immediate device area. The geometry size is such that electron-beam (e-beam) lithography is not required. The structure is dc isolated from either port and to the gate. Since the channel and gate electrodes are separate and isolated from the input/output ports, the device can be operated from positive or negative bias. The simplified model of this structure indicates it should have higher figure of merit than FETs plus the above advantages. A patent has been applied for this CFET structure, more descriptively referred to as a back-gate FET (BGFET).

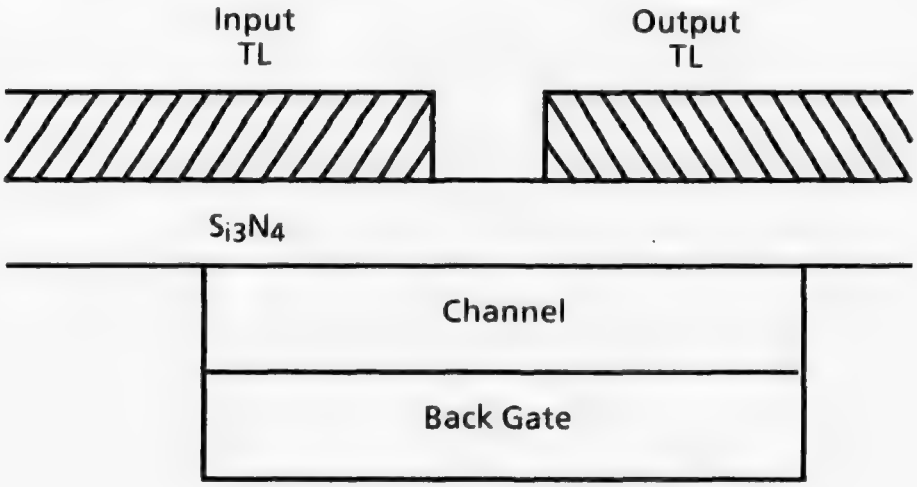

Figure 2-9. Back-Gate FET Cross Section

2.1.3 Summary/Conclusions

The preceding evaluation of the intrinsic parameters of various control elements clearly indicate two conclusions:

1. All of the control devices evaluated are dominated by parasitic elements, namely contact resistance.
2. PIN diodes have the highest figure of merit.

PIN diodes offer the highest figure of merit both intrinsically and extrinsically. Results from the NRL PIN diode switch development program have shown that a figure of merit exceeding

2,000 GHz has been achieved. The major disadvantages of PIN diodes is the operating current and bias circuitry required. The latest rf results from PIN diodes indicate that the operating current can be reduced to a few milliamps. The bias circuitry required to properly bias the PIN diode can be a problem, but the circuit design should be focused on the topology that allows easy integration of these bias elements. Figure 2-10 is a tradeoff matrix for each of the control devices with respect to various design and process parameters.

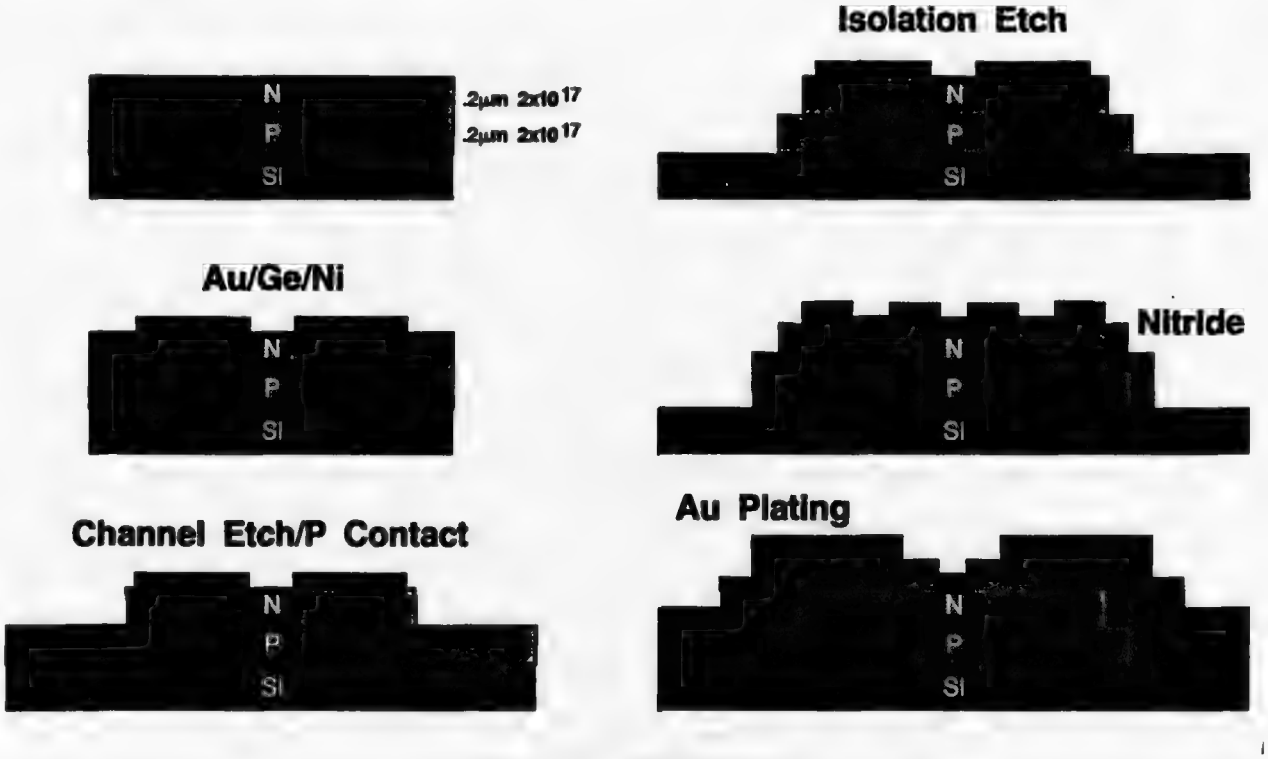

Figure 2-10. CFET Process

2.2 STRUCTURE

2.2.1 Cross Section

To improve the figure of merit for a control device, the on-resistance and/or the off-capacitance must be reduced. The CFET device, shown in cross-section in Figure 2-11, achieves both of these improvements by removing the gate from the conventional position on top of the channel and placing it beneath the channel. Removing the gate structure from the top surface of a typical MESFET eliminates the depletion capacitance that exists under the gate in the active layer. It also permits the source and drain contacts to be moved closer together, resulting in lower resistance.

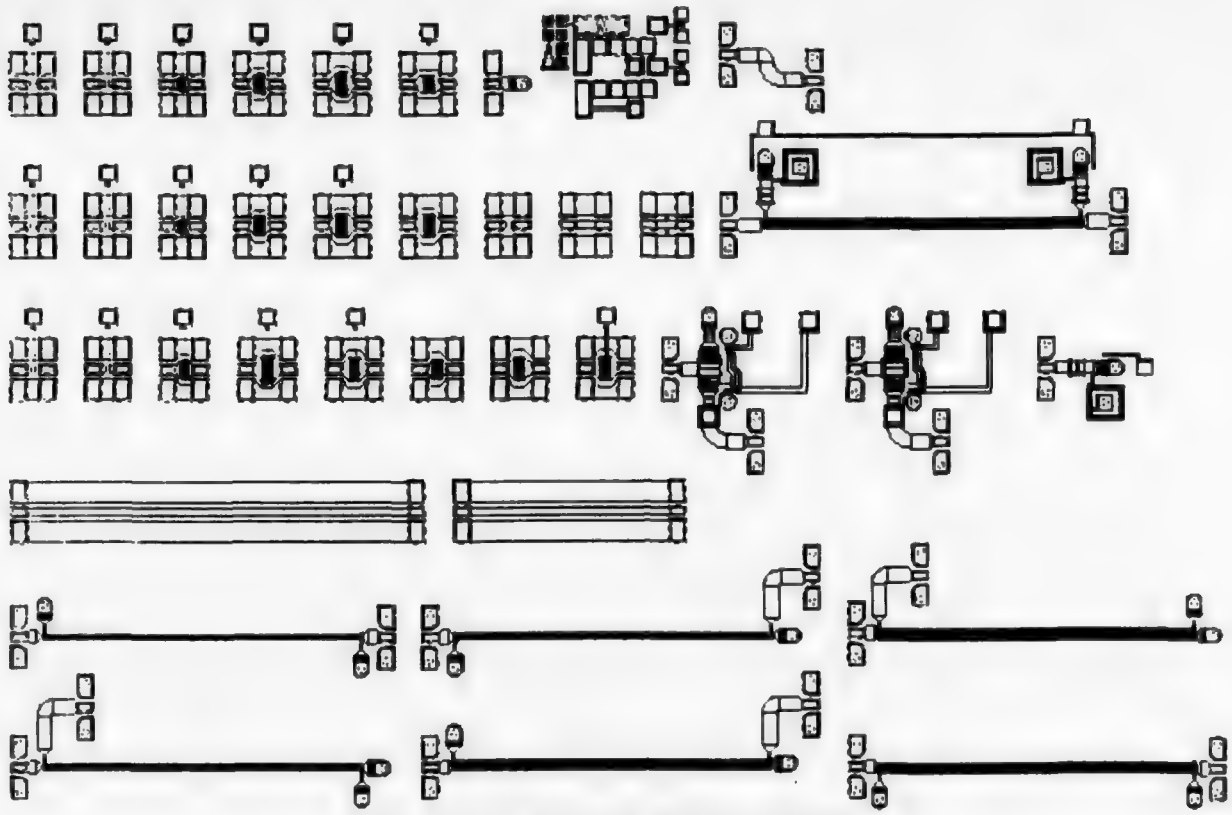

Figure 2-11. First Test Structure Layout

2.2.2 Material Parameters/Process Flow

The fabrication of the CFET is compatible with most of the same processing steps as for the MESFET. The geometry of the CFET is such that with the proper material layers, submicron lithography is not required, and thus, it is a simpler structure to fabricate.

The CFET process begins with an epitaxially grown structure shown in Figure 2-12. The n- and p-layer doping and thickness are carefully controlled so that full depletion of both layers is achieved at pinch-off. Measurements have shown that the off-capacitance of the device is the same as for an interdigitated capacitor on a semi-insulating substrate. Since the CFET does not have the additional depletion capacitance of typical MESFETs, the off-capacitance is significantly improved. 3-D electromagnetic modeling of the electrode structure has been done to minimize this off-capacitance and will be discussed later.

The first process step in fabricating CFETs is formation of the Au/Ge ohmic contacts, which is the same as for MESFETs. The ohmic contacts, or source-drain contacts, can be spaced as close as the optical lithography will allow. CFETs have been made with source drain spacing of 1.25 μm.

The n-layer is etched outside of the device area down to the p-layer. This etching isolates the CFET from each other. The p-layer is then defined and etched to provide a resistive extension for the CFET gate contact. The resistance of this p-region serves the same function as the gate resistor in a MESFET control element, mainly to isolate the rf from the dc bias line.

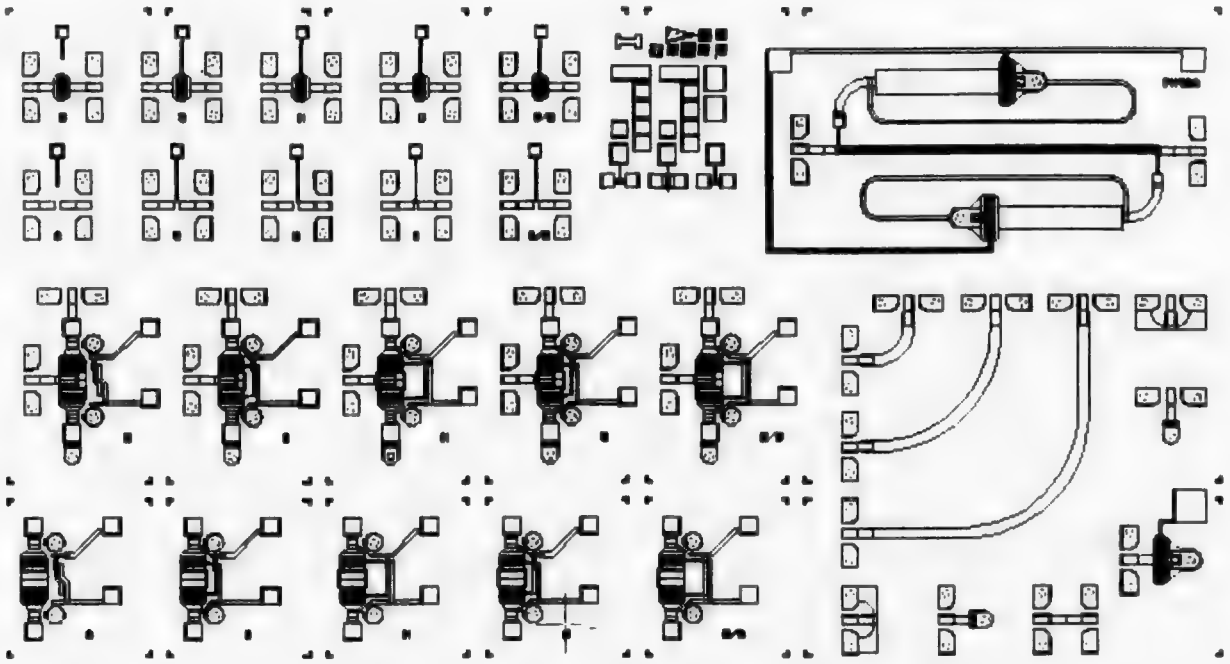

Figure 2-12. Second Test Structure Layout

The p-layer is contacted by the first-level metal. This quasi-ohmic contact allows positive bias on the gate with little bias current to be drawn even with +10 volts. Since the pn junction has a higher built-in potential than the Schottky diode of the MESFET, some positive bias on the gate increases the performance of the CFET. However, this requires no bias current, which is different from the current required for a MESFET. The transmission lines, capacitors, and other components of the MMIC are processed by the normal MESFET process and are not discussed here.

2.2.3 Test Structure Mask Set

Figure 2-11 is a layout of the first test mask used on this program. It contained various sizes of individual CFETs (50 to 800), Lange couplers for the reflective bits, two SPDT switches, and a 90-degree phase shifter bit. This test structure mask set helped to pinpoint the bias interaction described in the Test Structure Summary Report. Based on these test results, a second test mask was designed. The layout is shown in Figure 2-12. It contains a row of 800 CFETS and a row of 75 CFETS, both used in the SPDT switch. As described in the Test Structure Summary Report, for each size CFET there were five different bias schemes:

1. Large gate resistor with quasi-ohmic contact
2. Small gate resistor with quasi-ohmic contact
3. Small gate resistor with ohmic contact
4. Ohmic contact and leads on nitride
5. Combination of 2, 3, and 4.

The mask set also contained the rf calibration structures and a 90-degree phase shift bit.

After comparing the rf data for the individual CFET with the measured and modeled results for the SPDT switch, it was decided to use bias scheme 3 as the reference for the remaining tests. This bias scheme eliminated the bias interaction and reduced the testing and modeling required. The remainder of the program concentrated on the 800-m CFET with bias scheme 3 to feed back results to the process to improve the device figure of merit.

2.2.4 Improved CFET Structure

Early CFET results indicated difficulty in IV control because of the low uniformity in the growth of the epitaxial layers. A recess step was added to improve the uniformity. The source-drain metallization was used as the etch mask. The etch undercut the source-drain metallization, however, and increased the on-resistance. An N+ layer was added to the structure to improve the ohmic contacts, which would be etched away in the "channel" area later during the recess step. An e-beam lithography step was added to recess the channel to eliminate the source-drain metallization undercut.

The quasi-ohmic contact to the p-layer was changed to a true ohmic contact using Au/Zn. This change, combined with shortening the gate resistor, eliminated the rf/dc bias interaction between the back-gate and the nearby transmission lines. The addition of the p-layer ohmic contact allows a p-channel FET (PFET) to be formed. This PFET can be used to evaluate the pinch-off characteristics of the p-layer. This structure allowed the parasitic elements R_x and C_x (see Section 2.3.3 on device modeling) to be reduced in the latter slices.

2.3 DEVICE OPERATION

2.3.1 Theory

The CFET operates like a MESFET in that it is a depletion mode FET. The CFET gate is a pn junction on the back side of the active layer, hence the name, back-gate FET. Referring to Figure 2-9, when zero or slightly positive voltage (<1 volt) is applied to the gate, the depletion layer from the pn junction is reduced to zero, and the channel resistance is a minimum. The channel resistance, which consists of the two ohmic contacts and the sheet resistance of the channel, is the R_{on} of the CFET. A slightly positive voltage is preferred because of the higher built-in potential of the pn junction compared to the potential of the Schottky junction of a MESFET.

To turn the CFET off, a negative voltage is applied to the gate. The magnitude of this voltage depends on the doping and thickness of the two layers. For an n-layer and p-layer doping of 2×10^{17} /cm^3 and 0.2-μm thickness the pinch-off voltage would be 6 volts. This is slightly higher by 1 to 2 volts than for a MESFET. This higher pinch-off voltage occurs because there are two layers, hence more charge, to deplete. If both layers are equal in charge, i.e., same doping-thickness product, both layers will simultaneously deplete. This makes the CFET essentially disappear, leaving only the source and drain metal electrodes remaining. Using the calculations from Figures 2-11 and 2-12, the figure of merit for a CFET should be 2.3 times that for a similar MESFET.

2.3.2 Device Characterization

The CFET was dc characterized during the process and then RF characterized and modeled. The results from the rf modeling was fed back to the process to correct any deficiencies in meeting the goals for the CFET. The RF characterization is discussed in Section 2.3.3.

The characterization of the CFET during the process was done at several steps. The first step was after the ohmic contacts and first mesa etch. The ohmic contact resistance and channel resistance was measured and compared to values normally achieved for this step. Ohmic contact resistance was good if it was below 0.3 ohm-mm. Few slices failed this parameter because of the n+ contact layer. The channel resistance was good if below 400 ohms/sq. This parameter varied significantly because of the different n-layer thickness and doping spread. It also varied because of the p-layer doping. The p-layer doping changed the zero-bias depletion layer, which modified the n-layer thickness and thus the channel resistance. Since there was no gate formed at this time the built-in potential was the effective gate bias.

The gate recess was the next step where the CFET was characterized. As opposed to the MESFET the CFET total IV characteristics could be evaluated since the CFET gate was on the back rather than deposited later. The CFET was recessed to a pinch-off voltage rather than a saturated current level, as with MESFET's. The target pinch-off voltage was 3 to 5 volts. This satisfies the typical system voltage supply requirement of -5 volts. The IV curves pinched off well at -5 volts, but because of the pinch-off voltage of the p-layer, the CFET required voltages exceeding -7 volts to completely pinch-off the p-layer during RF test.

When the p-layer test structure became available, the PFET pinch-off voltage was also monitored. It was a function of the p-layer parameters and could not be varied by the recess step. Early in the process development the p-layer pinch-off was well in excess of the CFET. This resulted in the high off-capacitance explained in Section 2.3.3.

The results from the p-layer test structure indicated the p-layer was too highly doped. The doping of the p-layer on subsequent slices was reduced from 2×10^{17} a/cm^3 to 1.5×10^{17} a/cm^3 and eventually to 1.2×10^{17}a/cm^3. This reduced the PFET pinch-off voltage from -7 to -3 volts, comparable to the CFET. This also reduced the parasitic off-capacitance from values as high as 0.15 pt to 0.008 pF on the better slices.

During the rf characterization CFETs with good pinch-off parameters (Ipo < 5 percent Ion) were chosen to be rf modeled. Because of the low uniformity of the material and recessing step, several slices had a large variability of pinch-off voltage across the slice.

RF results were averaged on the CFETs that represented the best fit to the average observed on each slice.

2.3.3 Device Modeling

A preliminary equivalent circuit model was derived for the CFET and compared to the typical MESFET. A cross-sectional view of both the CFET and a standard FET are shown in Figures 2-13 and 2-14. The channel on-resistance is calculated using the known doping

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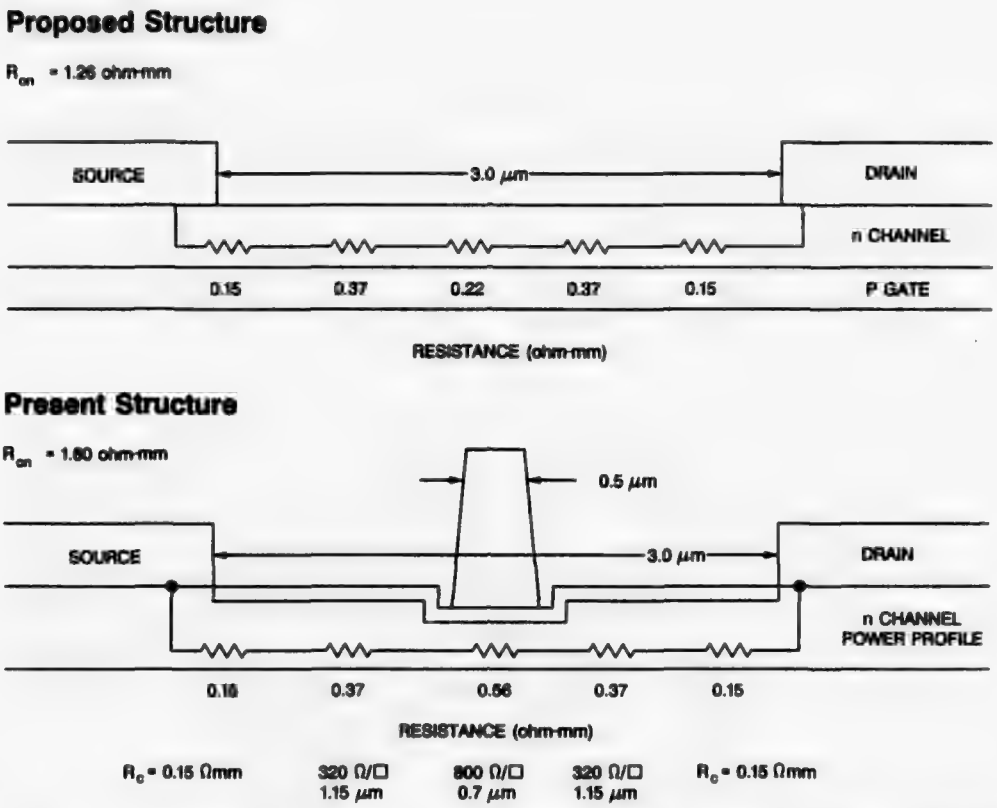


Figure 2-13. Comparison of CFET and Standard FET Models for On-Resistance Calculation

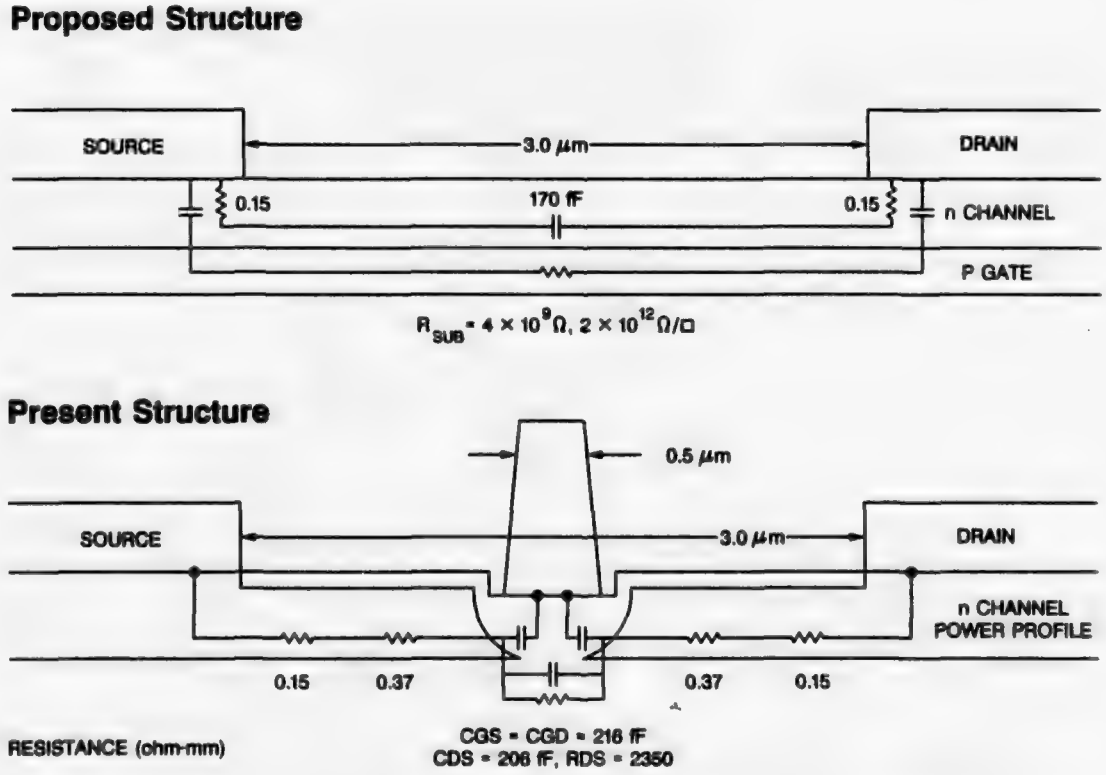


Figure 2-14. Comparison of CFET and Standard FET Models for Off-Capacitance Calculation

concentrations, and the off-capacitance is calculated using electromagnetic simulations. The predicted CFET figure of merit, or sometimes referred to as cut-off frequency) is over twice that of the MESFET. Measured device characteristics have confirmed a FOM 2 to 2.5 times that of the 0.5-μm MESFET.

Modeling of the CFET layout was done to determine the optimum interdigitated structure. The off-capacitance of the CFET is determined almost entirely by the electrode geometry. Measurements made on the original slice of CFETs both with, and without, active area show that the capacitance of CFET is dominated by the metallization pattern. Modeling of the original device has been performed on both LIBRA and SONNET. SONNET is a 3-D electromagnetic simulator and is ideal for analyzing metallization patterns from physical layouts. Using both LIBRA and SONNET, an improved electrode structure has been designed. Both the original and improved CFET structures are shown in Figure 2-15. Table 2-1 lists the modeled and measured resistance and capacitance for the two geometries. The improvements suggested by the SONNET modeling predicted an increase in device FOM of about 40 percent (from 550 to 770 GHz).

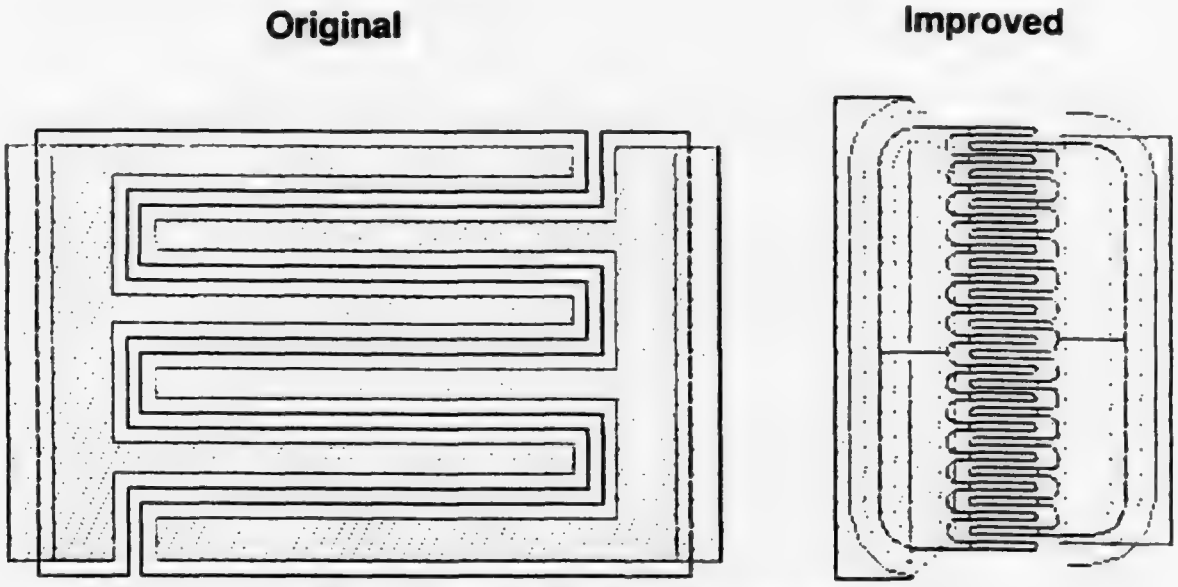


Figure 2-15. Original and Improved CFET Structure

TABLE 2-1. COMPARISON OF ORIGINAL AND IMPROVED CFET PARAMETERS

Parameter	LIBRA	SONNET*	Measured
Original BGFET capacitance	0.042 pF	0.041 pF	0.048 pF
Improved BGFET capacitance	0.03 pF	0.028 pF	
Original BGFET resistance		5.6 Ω	6 Ω
Improved BGFET resistance		5.3 Ω	
Original BGFET f_c		693 GHz	553 GHz
Improved BGFET F'		1,073 GHz	

*Contact resistance of 1.3 Ω added, was not included in SONNET analysis.

The 800-μm CFET from the test structure mask layout (see Section 2.2.3) was chosen as the element to determine the rf model. S-parameters were measured from 0.5 to 25 GHz. These S-parameters were used to arrive at an equivalent circuit model, shown in Figure 2-16. The resistance and capacitance values were optimized to obtain a best fit across the frequency band. The resistance-capacitance (RC) model is the same as a MESFET with two additional elements, R_x and C_x. These elements, which represent the parasitic components associated with the undepleted p-layer, degrade the figure of merit of the CFET. Table 2-2 shows the major element components of all of the slices tested.

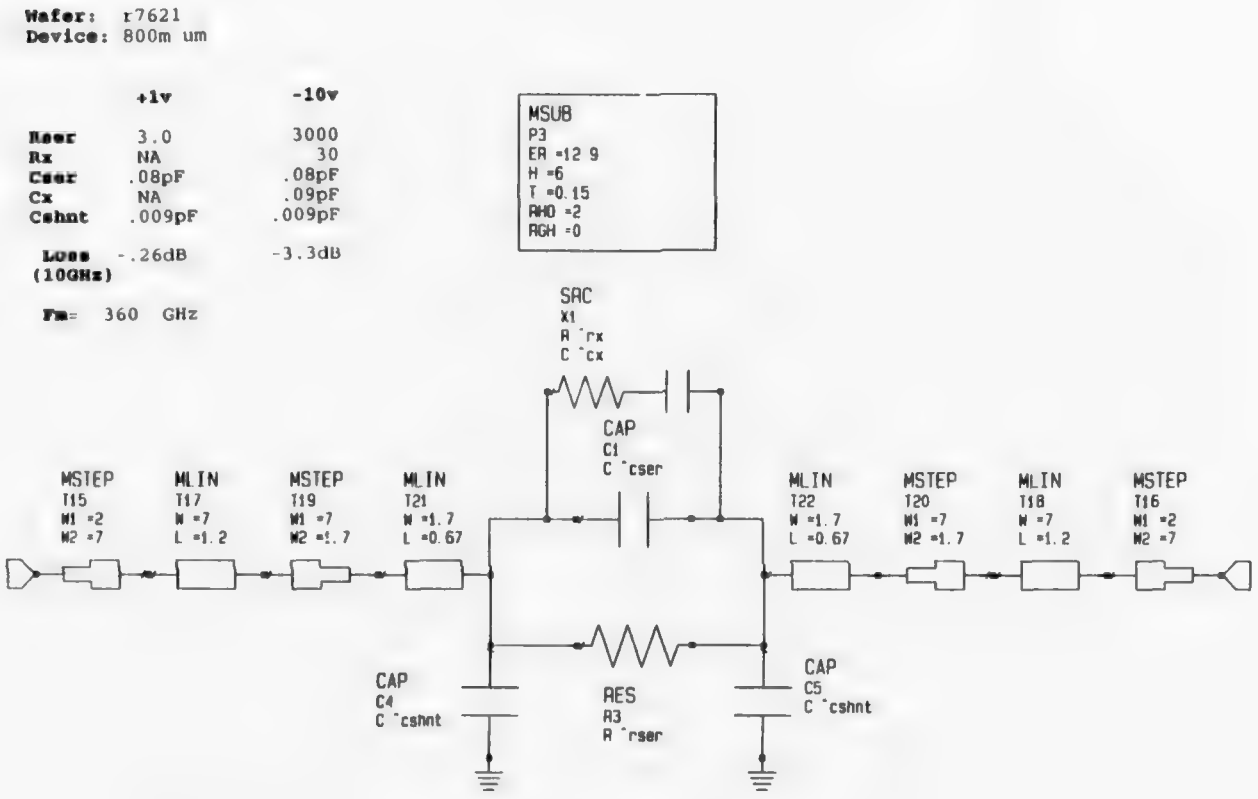


Figure 2-16. CFET Equivalent Circuit Model

2.3.4 Recommended Operating Conditions/Limitations

The operating conditions for the CFET are similar to the MESFET in that the CFET requires zero or slightly positive (<1 volt) voltage to turn on. The turn-off voltage is negative and is larger for the CFET. The pinch-off voltage is larger for the CFET, for two reasons. The main reason is that two layers are required to be depleted rather than the one for a MESFET. The other is the p-layer doping-thickness product has to match the n-layer to pinch-off simultaneously. Excess p-layer doping-thickness product requires a larger pinch-off voltage to fully deplete the p-layer. Early slices with high p-layer doping would not pinch-off during rf characterization until -10 volts was applied. RF characterization was done at -5 and -10 volts to evaluate the off-capacitance. These characteristics were compared to the dc pinch-off voltage, which gave an indication of the p-layer pinch-off voltage. Later slices with the p-layer test structure allowed direct correlation with the rf measurements.

TABLE 2-2. SUMMARY OF CFET SLICES

WAFER	R_{ON} (ohms)	Cser (pF)	Rx (ohms)	Cx (pF)	C_{OFF} (pF)	Fm (GHz)
6298	3.0	0.065	0	0	0.065	816.2
6789	16.0	0.100	0	0	0.100	99.5
6790	3.5	0.055	120	0.15	0.135	336.8
6871	5.0	0.065	120	0.18	0.141	225.7
7041	7.0	0.065	235	0.09	0.103	219.3
7172	3.5	0.065	80	0.17	0.157	289.6
7173	3.3	0.065	60	0.24	0.191	252.5
210-1221	13.5	0.065	600	0.017	0.075	156.4
210-1222	9.0	0.065	180	0.07	0.103	170.2
210-1224	4.8	0.065	250	0.15	0.109	302.3
7234	8.5	0.065	400	0.035	0.084	223.9
7335	4.2	0.065	35	0.170	0.228	165.8
7336	3.2	0.065	00	0.05	0.103	482.7
7410	5.0	0.080	30	0.09	0.156	202.8
7423	3.1	0.080	30	0.08	0.150	343.4
7424	3.6	0.080	90	0.05	0.120	371.6
7561	2.4	0.080	30	0.08	0.150	443.5
7563	5.0	0.080	10	0.44	0.344	92.3
7565	3.0	0.080	70	0.11	0.154	344.2
7613	5.2	0.080	30	0.07	0.157	207.0
7620	2.4	0.080	30	0.08	0.149	442.0
7621	3.0	0.080	30	0.09	0.162	360.0

In the on-state usually a +1 volt was applied. CFETs with the quasi-ohmic contact to the p-layer would not draw gate current since the quasi-ohmic contact was reversed biased, allowing only leakage current to flow. CFETs with the Au/Zn p-layer ohmic contact biased positively would draw gate current. The current would however be limited by the 2 to 5 Kohm gate resistor. This would be the same operating condition as for a MESFET with a positive gate bias.

The breakdown voltage of the CFET from gate-to-drain/source was that of the pn junction. Since the voltage was spread over a larger distance of two layers, the electric field for a given voltage was lower. This allowed a larger breakdown voltage of over 20 volts.

The breakdown voltage of the CFET was limited by the reach-through voltage from source to drain. The depletion layer with applied voltage would spread from the drain until it reached the source. The spacing and doping of the source-drain contacts determine the source-drain breakdown. The breakdown for a 2.5-μm source-drain spacing was 8 to 10 volts.

When the source-drain spacing was reduced to 1.5 μm, the breakdown voltage was reduced to 6 to 7 volts. The breakdown voltage of the 2.5-μm source-drain spacing of 10 volts would permit operating power levels up to 27 dBm. RF power tests on the SPDT switch confirmed these results.

SECTION 3
PHASE SHIFTER

3.1 BACKGROUND OF PHASE SHIFTER DESIGN

A listing of significant microwave phase shifter development efforts carried out at Texas Instruments since 1972 is provided in Table 3-1. This work was carried out in frequency bands extending from S-band to Ku-band using both FETs and PIN diodes as control elements. The work conducted before 1986 employed discrete control devices embedded in transmission lines of stripline or microstrip form, while work conducted after that period used monolithic circuit technology employing the microstrip transmission line configuration. While all the early work was designed to fulfill narrow frequency band requirements, work in 1992 was initiated to develop a very wide band (3:1 frequency band) 6-bit phase shifter. The work in place at that time was well aligned with the needs of the NRL wide band phase shifter program. The goals of the program are shown in Table 3-2.

TABLE 3-1. PHASE SHIFTER DEVELOPMENT AT TEXAS INSTRUMENTS

Year	Program	Bits	Frequency (GHz)	Loss (dB)	From
1972	MEWS	3	2.5 to 5.0	5.0	Switched lines on Al_2O_3 (PIN)
1974	AESPA	3	S-band	3.0	Switched lines on Al_2O_3 (PIN)
1975	NRL	3	2.0 to 8.0	10.0	Switched lines on Al_2O_3 (PIN)
1976	TMLS	4	C-band	2.7	Reflective bits on stripline (PIN)
1984	DARPA	4	X-band	8.0	Switched lines on GaAs (FET)
1986	SSPA	5	X-band	5.0	Switched/loaded lines on Al_2O_3 (PIN)
1987	ManTech	6	X-band	7.0	Switched/loaded lines on GaAs (FET)
1988	Sandia	4	Ku-band	6.0	Switched lines on GaAs (FET)
1989	PM-1	3	X-band	3.0	Switched/loaded lines on GaAs (FET)
1990	OST	6	X-band	6.0	Switched/loaded lines on GaAs (FET)
1990	F-22	6	X-band	4.0	Switched/loaded/reflective (FET)
1992	Wideband	6	6.0 to 18.0	10.0	

TABLE 3-2. WIDEBAND PHASE SHIFTER GOALS

Parameter	Goal
Frequency (GHz)	6 to 18
Insertion loss (dB)	8.5
RMS phase error (degrees)	10
Switching time (nS)	50
Control voltage (V)	-10, +3
Control current (μm)	10/bit
Maximum chip size (inch)	0.080 × 0.150
Input/output VSWR	<2.0:1
TOI at input (dBm)	>20

Phase shifter forms that have been used successfully for 3:1 frequency band operation are shown in Figure 3-1. The top two, the switched filter and integrated high-pass/low-pass, are realized by switching the control elements to select either a low-pass or high-pass filter configuration. Use of the low-pass filter retards the phase, while use of the high-pass filter advances the phase. The switched filter approach accomplishes this by choosing the filters using two single-pole/double-throw (SPDT) switches, while the integrated high-pass topology accomplishes this by changing the complete structure from low-pass to high-pass form using control elements that are embedded in the filters themselves. The lower three phase shift forms of Figure 3-1 were being used successfully in a wideband phase shifter under development at the time this program was initiated. The switched coupler bit form, shown on the left, can be thought of as using either shorted or open-circuited quadrature directional couplers as reflective loads that are selected by SPDT switches. The open-circuited coupler is usually replaced by a filter that is the dual of the shorted coupler. This form is employed in the realization of the 180-degree bit. The reflection type circuit, shown at the lower-center, is a reflective bit that is realized by employing the control element and its proper matching structure as loads for the quadrature directional coupler. Although this form can be used for any of the phase bits, its use was limited to the 45- and 90-degree bits. The final form shown on the lower-right is a loaded-line form that was used on the three smallest phase shift bits. In this form the phase is varied by choosing either a series capacitor or inductor (realized using a high impedance transmission line) by shorting out the undesired element using an FET. The expected performance of various phase shifter forms in the band of interest is shown in Table 3-3.

The wideband phase shifter developed on the MIMIC program (EG6335) employing integrated high-pass/low-pass bits for the three largest bits and loaded-line bits for the smallest

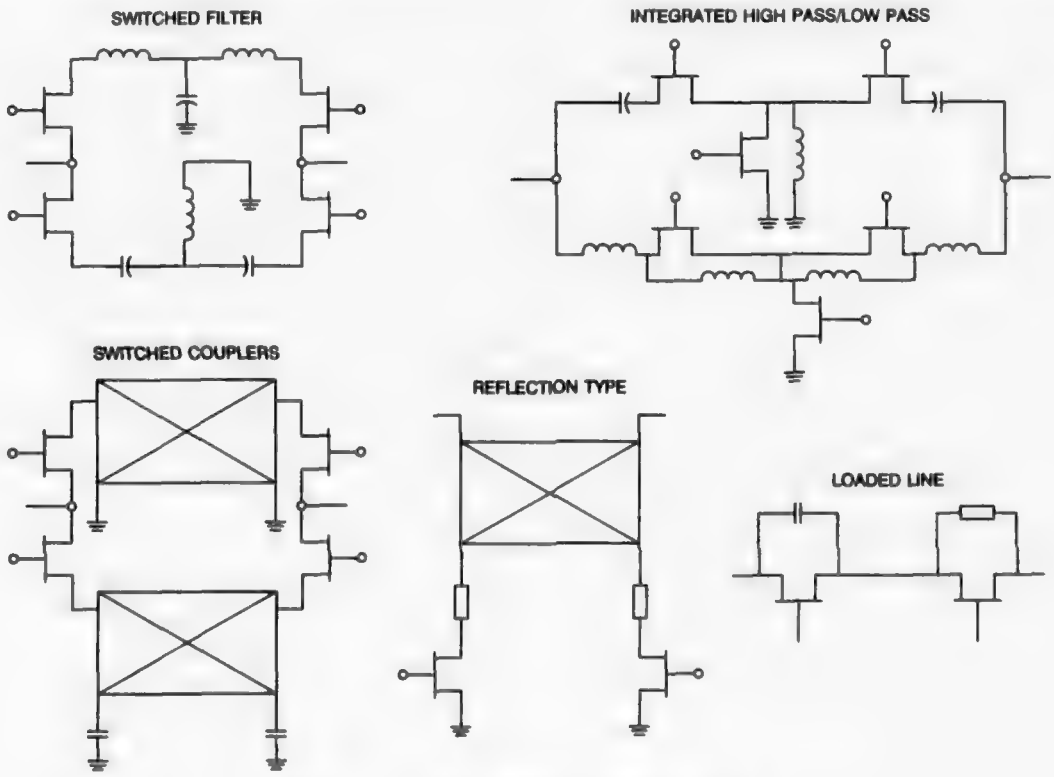


Figure 3-1. Phase Shifter Configurations

TABLE 3-3. WIDEBAND PHASE SHIFTER BIT COMPARISON
Frequency Band 6.0 to 18.0 GHz

Phase Shifter Bit Form	Loss (dB)	VSWR	Phase Error	Size (mils)
180-degree bit				
Switched couplers	2.1	2.5	-3/+3.8	65 ×150
Switched filters with embedded FETs	2.2	2.3	±15.0	26 × 40
Reflective	1.9	2.0	±2.5	75 × 150
90-degree bit				
Switched filters with embedded FETs	1.4 to 2.6	2.5	±10.0	70× 80
Reflective	0.7 to 3.0	1.8	±1.0	40 × 118
45-degree bit				
Switched filters with embedded FETs	0.7 to 1.5	2.3	±5.0	45 × 50
Reflective	0.8 to 2.2	1.7	±1.0	40 × 118
22.5/11.25/5.625 loaded-line bits				
22.5	0.4 to 2.2	2.2	-1.0/+1.8	20 × 20
11.25	0.35 to 0.80	1.5	-1.0/+1.2	15 × 20
5.625	0.25 to 0.50	1.2	-0.4/+0.9	15 × 20

bits, was originally considered for use in this wideband phase shifter application. Its use was abandoned when it was determined that the RMS phase error was greater that 15 degrees in the band of interest. A photograph of this phase shifter chip is shown in Figure 3-2. This phase

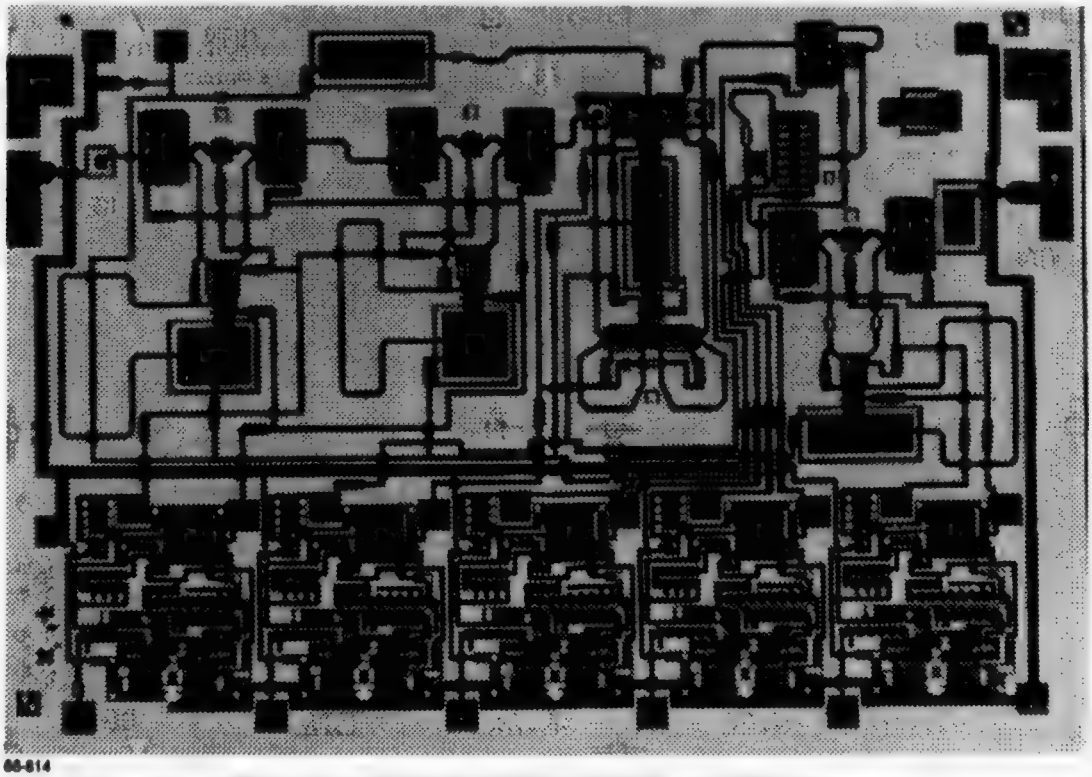


Figure 3-2. EG6336 MIMIC 5-Bit Phase Shifter

shifter loss performance was estimated for FET control elements of varying quality and the results are shown in Table 3-4. This table serves to provide a history of device quality that has been available to the designer and to demonstrate the advantage afforded by use of the CFET possessing the quality that it promises to provide.

TABLE 3-4. EG6335 LOSS VERSUS CONTROL ELEMENT PERFORMANCE

Date	Program	F_c (GHz)	FET Loss (dB)	Chip Loss (dB)
1985	DARPA	165	16	18
1991	Gen-X	246	11	13
1989	EG8407/EG8424			
	3.0 μm S-D	288	9	11
	2.5 μm S-D	332	8	10
1992	CFET	700	5	7

3.2 PHASE SHIFTER DESIGN WITH CFET

After conducting the necessary performance trade studies of phase bits of the quality listed in Table 3-3 the final mix of phase shift bits comprising the chosen form of the six-bit phase shifter are listed in Table 3-5. The estimated performance of this configuration is shown for implementation of ion-implanted FETs having a source-drain spacing of 2.5 μm.

TABLE 3-5. WIDEBAND PHASE SHIFTER BIT CONFIGURATION
Frequency Band 6.0 to 18.0 GHz

Phase Bit		Loss (dB)	VSWR	Phase Error	Size (mils)
180	Switched couplers	0.8 to 2.1	2.1	-3.0/+3.8	65 × 150
90	Reflective	0.7 to 4.0	1.8	-1.0/+1.0	118 × 140
45	Reflective	0.8 to 2.2	1.7	-1.0/+1.0	118 × 140
22.5	Loaded line	0.4 to 2.2	2.2	-1.0/+1.8	20 × 20
11.25	Loaded line	0.4 to 0.8	1.5	-1.0/+1.2	15 × 20
5.625	Loaded line	0.3 to 0.5	1.3	-0.4/+0.9	15 × 20
	Total	4.9 to 9.6	2.8	1.7 to 4.0 RMS	250 × 140
Ion-implanted FET (2.5-μm source-drain spacing)					

A layout of this phase shifter is shown in Figure 3-3. When the ion-implanted FETs in this phase shifter are replaced by CFETs scaled to the same capacitance value the predicted insertion loss is reduced by approximately 1.5 dB. Table 3-6 is a list of estimated loss improvements expected for each of the phase shift bits. It is noted that the loss improvement is greatest for the larger phase bits. The differential phase, insertion loss, and return loss for each

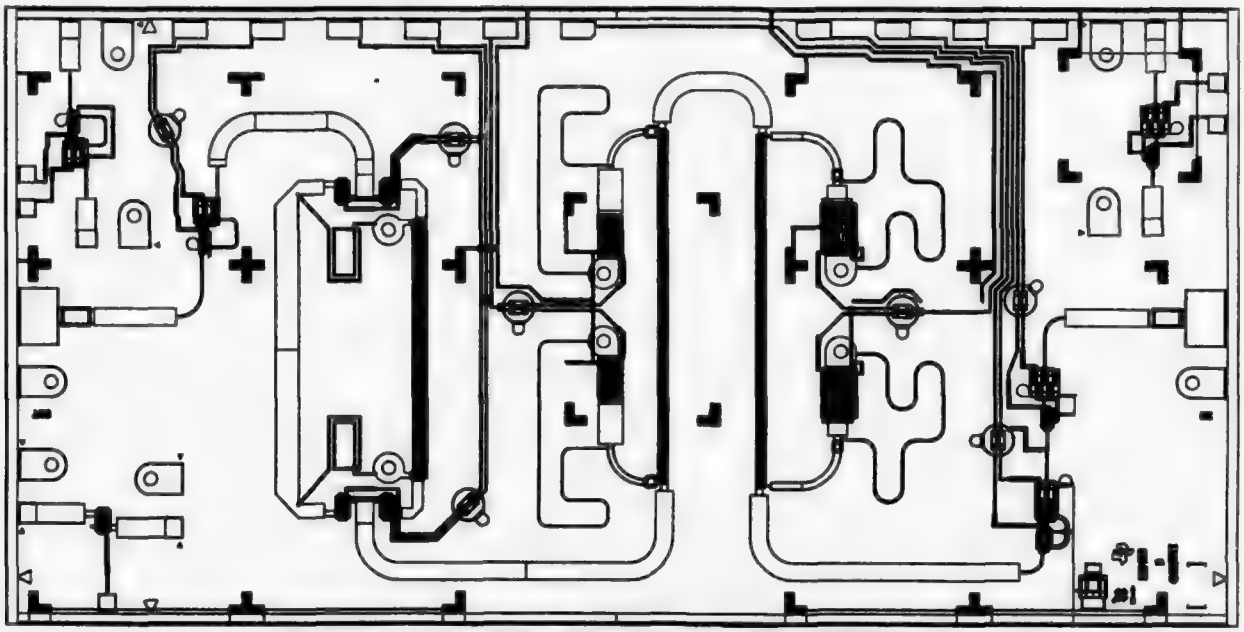


Figure 3-3. EG6450 6-Bit Wideband Phase Shifter

of the phase bits employing CFETs was obtained using the EEsof Libra CAD software. This predicted performance summary is provided in Appendix A.

TABLE 3-6. LOSS IMPROVEMENT

Phase Bit	Loss Imrpovement (dB)
5.625	0.05 to 0.10
11.25	0.10
22.5	0.05
45	0.2
90	0.3
180	0.75
Total	1.5 dB
CFET Size = 2.8 × FET	

Subsequent to the trade study described above the selected phase shifter form employing ion-implanted FETs was fabricated as part of another program (EG8430b) and evaluated. Work on the 45-and 90-degree reflection-type bits revealed them to be more sensitive to load parameters than was initially anticipated. Results achieved with bits of this form have led to the discovery that errors in FET off-state capacitance, metal-insulator-metal (MIM) capacitor values, and via inductance have been significant enough to cause large errors in phase shift. Although these errors were eventually thought to be well understood, efforts to develop an alternate phase shift form for these bits were undertaken. One form considered employs all-pass and high-pass filters that are switched by use of SPDT switches. Traditionally a combination of high-pass and

low-pass filters are used to implement a switched filter phase shifter. A form of these filter structures that could be realized in microstrip transmission-line form was conceived. Each of the phase bits is composed of one seven-element high-pass filter, one all-pass filter of order 2 and two SPDT series-shunt CFET switches. These structures are shown schematically in Figure 3-4. Predicted performance obtained for the 45-degree bit is compared to the performance of the reflected bit configuration in Figure 3-5. The predicted switch loss in the 3:1 frequency band centered at 12 GHz is approximately 0.75 dB. The total loss of the switch filter configuration is approximately 0.5 to 1.0 dB greater that predicted for the equivalent reflective bit configuration. Similar phase error and VSWR performance is predicted for the two phase shift forms.

The EG8430b wideband phase shifter (revised and renamed the EG8450) that implemented ion-implanted FETs with 2.5-μm source-drain spacing was chosen as the desired component for use in evaluation of the CFET device. Because of the problems encountered in fabricating CFETs that were reproducible and of good quality it was felt that the best interests of the program would be served by fabricating and evaluating the phase shift bits as individual components. This would make it possible to more easily separate device and circuit design problems. Work on this effort to implement the new device started with a decision about the expected CFET model. A comparison of measured CFET and ion-implanted models obtained at the beginning of this program is shown in Figure 3-6. Since the completion of that work, efforts to improve and reproduce the devices have been of major importance. During the course of that activity the CFET quality was seen to vary from cut-off frequencies of 150 to over 450 GHz. At the start of this phase bit design activity the device quality was seen to be improving, and it seemed reasonable to assume that the quality and reproducibility would reach a level that would make our quest for component loss improvement successful. Based on recent device results we

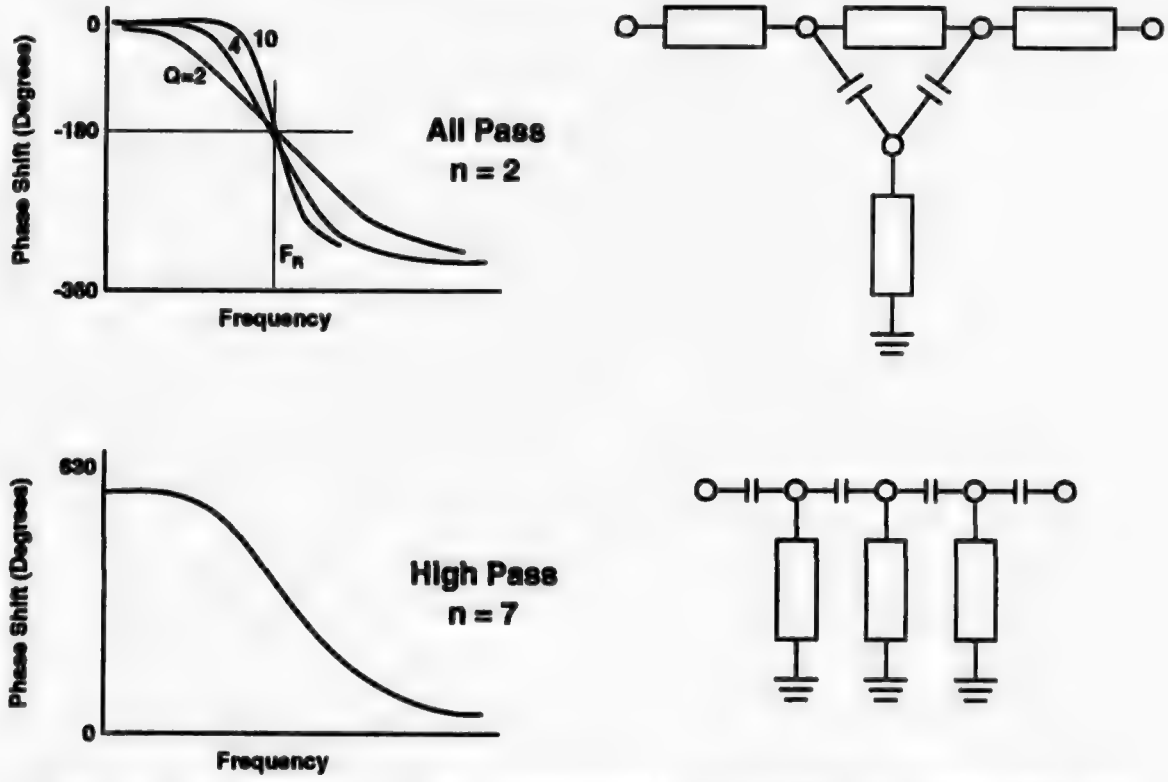


Figure 3-4. Configuration and Phase Characteristics of All-Pass/High-Pass Phase Shifter Bits

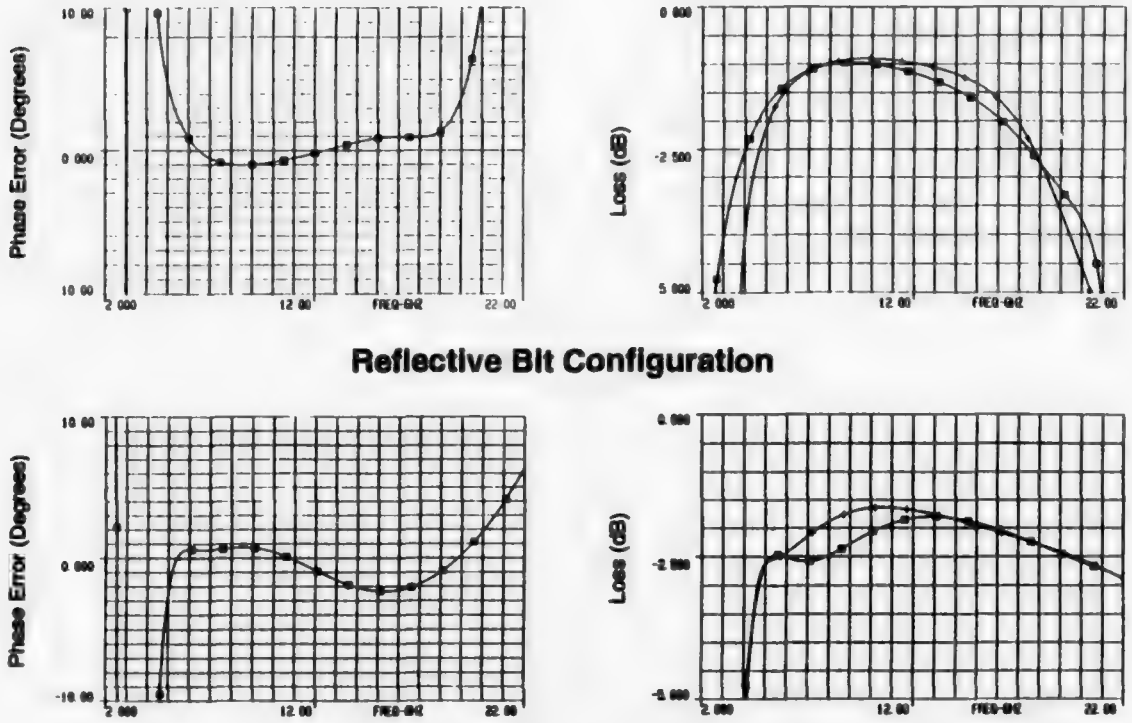


Figure 3-5. Predicted Performance of Two 45-Degree Phase Bit Forms

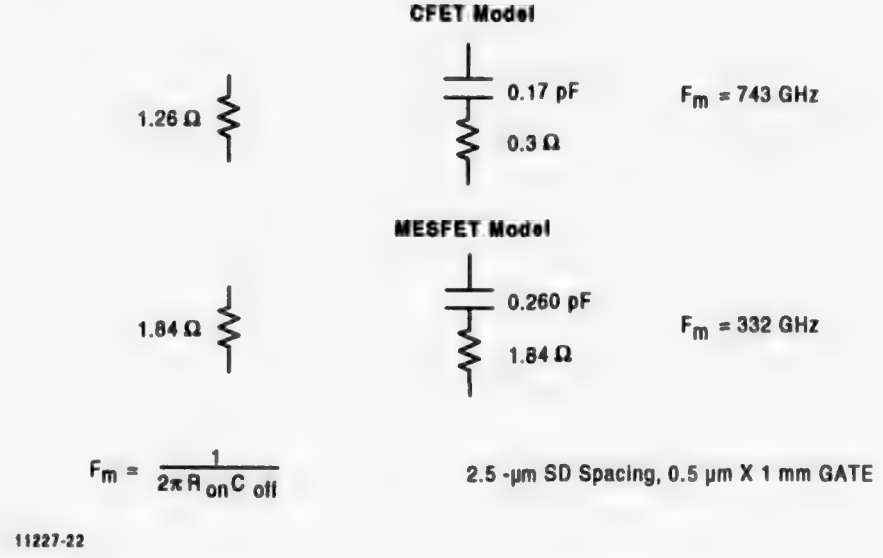


Figure 3-6. Control Element Comparison

decided to design the phase shift bits based upon an anticipated device cut-off frequency quality of 600 GHz. The configuration of CFETs that were appropriate for replacement of the ion-implanted FETs that were in use was determined. The minimum finger length used was increased from 2.5 to 7.5 µm and the number of fingers and finger width were altered to permit device replacement with no tuning adjustments required. The CFETs that required the use of

capacitors on the fingers were also altered to incorporate this feature. Phase shift bits incorporating these CFETs were removed from the EG8450 6-bit phase shifter mask and placed on the new mask for individual evaluation. Also included on this mask were the new switched high-pass/all-pass 45-and 90-degree bits, and rf probable forms of all the CFETs that were modified for use on the individual bits. A layout of all the test elements provided for evaluation is shown in Figure 3-7.

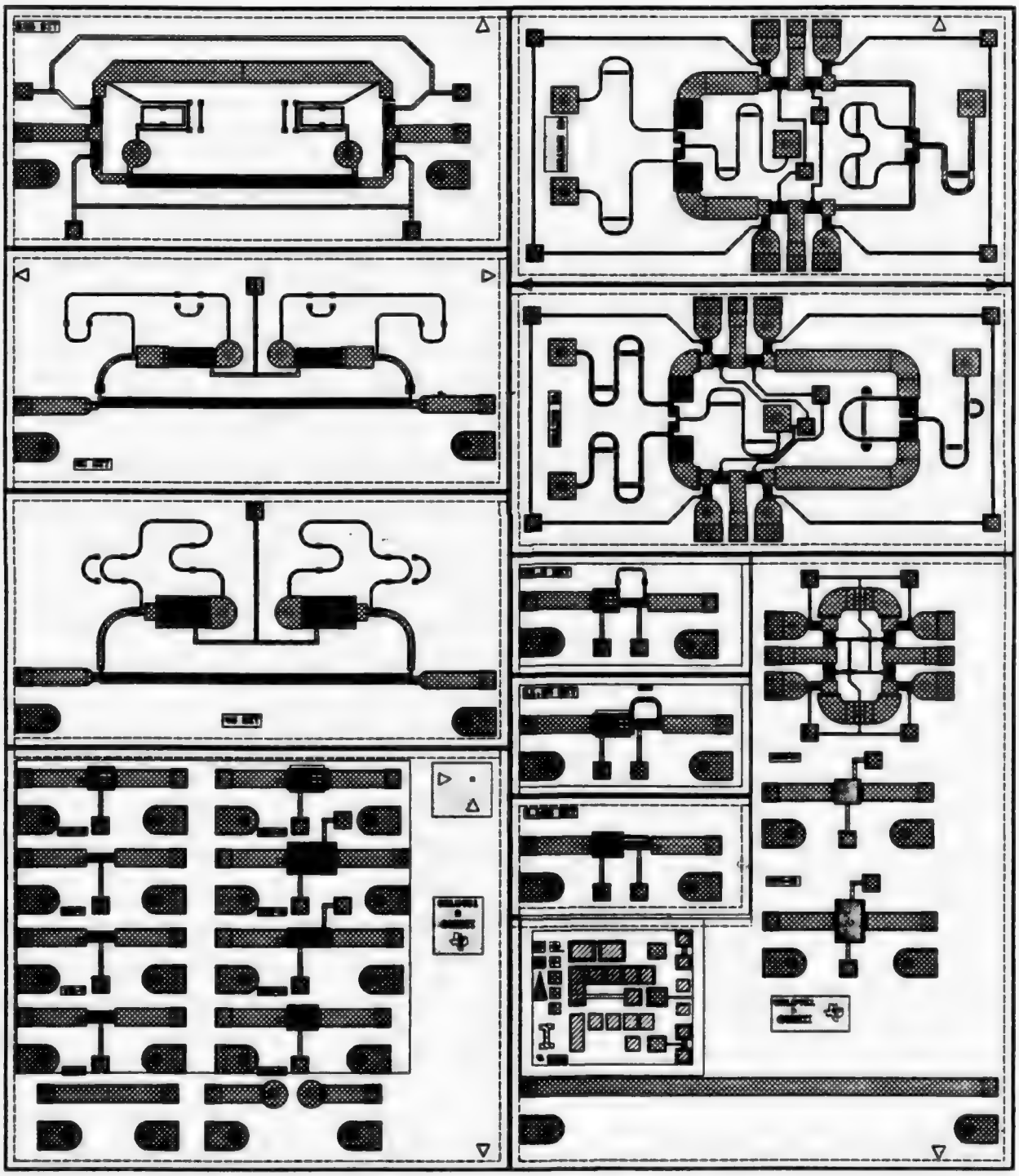


Figure 3-7. Layout of CFET Phase Bits and Test Structures

One slice of the newly design phase bits and devices was available for test during the course of this program. Evaluation of the devices revealed that the devices failed to provide the level of performance expected. Figure 3-8 shows the comparison of the measured model and the model used for design of the components. The results indicate that the cut-off frequency is about one-third the value anticipated. In addition the forward resistance is twice as much as expected, and the reverse capacitance is 50 percent greater that expected. The increase in resistance results in greater loss of each bit than expected, while the increase in capacitance results in deviation from expected phase performance. The measured phase shift performance of the individual phase bits is provided in Appendix B. Because of metal lift-off problems occurring on the large FETs the reflection-type 45- and 90-degree bits failed to perform in a predictable manner. For the remaining phase bits, insertion loss, phase shift, and return loss performances are shown for three conditions: (1) projected performance using the ideal FETs with 600 GHz cut-off frequency, (2) projected performance using measured FET S-parameters from the slice, and (3) measured phase bits performance from the slice. As expected from the lower-than-expected CFET figure of merit, agreement between the original analysis (using ideal FETs) and the measured performance is very poor. In most cases, however, the measured performance and analyzed performance (using measured FET parameters) is much better.

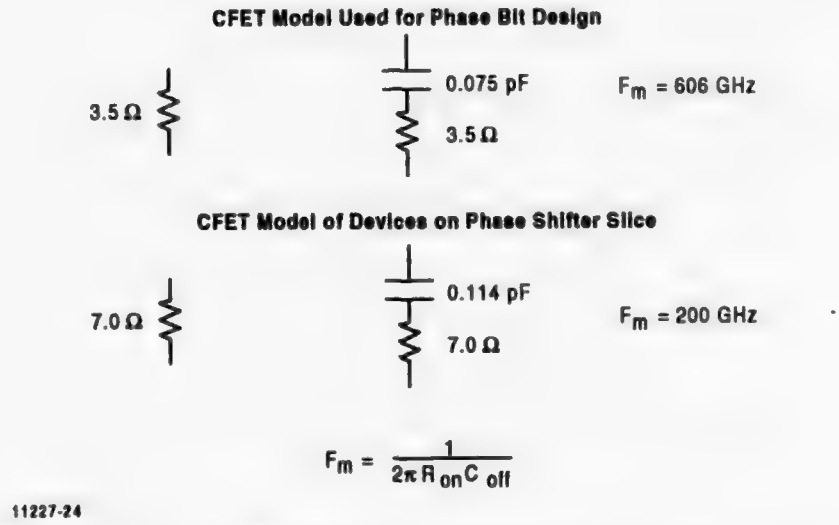


Figure 3-8. Achieved/Predicted Control Element Performance

Although it is disappointing that the desired level of device performance has not yet been achieved on this program it is significant that we have made use of the devices in a phase shifter design that exhibits good performance with minimum design modification to the basic circuit configuration. The stage has been set for easy implementation of the CFET device if further work proves to yield the desired device quality. It is also significant that a new form of switched filter phase shifter bits using all-pass/high-pass filters has been successfully demonstrated. Although these phase bits appear to exhibit more loss than the reflective configurations of the same differential phase, they are thought to be more reproducible. The bits did prove to function in a predictable manner, thus enabling us to successfully demonstrate phase bits of all the desired phase shift values.

SECTION 4
CONCLUSIONS

4.1 PROGRAM SUMMARY

4.1.1 Highlights

To achieve the goals of this program two tasks had to be accomplished: (1) CFET development and (2) phase shifter circuit design.

Clearly the circuit design of the phase shifter would meet the goals of this program if the CFET had been developed to its full potential. A study was made of phase shifter topologies, and the optimum mix of these topologies was chosen to meet the goals. In addition, a new phase shift bit topology, the all-pass/high-pass filter approach, was evolved on this program and proved to be a suitable alternative to the conventional phase shift topologies.

Conceptually the CFET structure was successful in making the gate capacitance disappear since the gate capacitance is a major portion of C_{off}. The structure eventually chosen enabled control of the IV characteristics by a recess step to overcome material growth problems. However, it was these material growth problems that limited the CFET performance. By using the inverted structure discussed in Section 4.3.1, the material problem would be reduced to just one side of the junction, the n-layer. The CFET allowed a new concept to be explored and to provide future opportunities for improved FET structures.

4.1.2 Disappointments

The inability of the CFET to repeatably achieve its early results was a major disappointment. Again, control of the material growth parameters was the key factor. Although the CFET achieved similar performance to 0.5-μm MESFETs, early results promised figures of merit exceeding 800 GHz. If these results could have been reproduced, clearly a new control element would have dominated the next generation microwave modules and systems.

4.2 LESSONS LEARNED

4.2.1 Material

Although the CFET structure is relatively simple, the requirement for both layers to simultaneously deplete proved difficult to achieve. This was the single most important parameter to control. Other effects such as surface depletion and substrate effects added to this control problem.

The surface depletion effect is caused by the charge at the surface of interface if a passivation dielectric is deposited. The effect is similar to the problems found early in the development of silicon MOS devices. The surface depletion layer reduces the channel thickness, increases the on-resistance, and decreases the CFET pinch-off voltage. This depletion layer is a function of the doping level, surface treatment, and surface passivation. This surface depletion layer is not well understood in III-IV materials, and is one reason why the p-layer doping was

reduced to match this decreased n-layer thickness. The p-layer thickness was reduced in a similar manner because of the substrate doping and associated depletion layer. This effect is more controlled and understood than the surface effect. However, it was a variable that was not comprehended in the original device design.

Present device modeling could predict the CFET sensitivity to epitaxial layer parameters but is not sophisticated enough to include the above effects. More process test structures developed early in the program would have helped determine the sensitivity of these effects. A well-planned design of experiments (DOE) would have been very helpful to isolate material (and processing) problems.

4.2.2 Processing

The initial process flow of the CFET was relatively simple compared to the MESFET. As problems were encountered, such as the undercut of the source-drain metallization, process steps such as e-beam lithography were added. The final process evolved to where it was as complex as a 0.5-μm gate MESFET. This would have been satisfactory if the CFET would have demonstrated a sufficiently larger figure of merit than the MESFET. Since the CFET FOM was comparable to the present 0.5-μm FET (higher in some cases) it would not justify the transfer of this technology to the GaAs production pilot line. The figure of merit would have to be twice as high as the MESFET to justify the expense of transfer to production.

4.2.3 Circuit Applications

Phase shifter circuit topologies were explored, and a hybrid mix was chosen to achieve the goals of this program. A design procedure for the reflective phase shift bits based upon a method proposed by Harry Atwater has been perfected. An alternate switched filter form has been developed and demonstrated on this program. This form alleviates the process variability of the coupler on the reflective phase shift bits.

4.3 CONCLUSIONS/RECOMMENDATIONS

4.3.1 Improved CFET

The concept of using a pn junction for the gate and having it essentially "disappear" by applying gate bias was correct. RF data indicates that the present CFET achieved at least equal performance with 0.5-μ gate MESFETs. The back-gate structure was chosen to allow control of the n-layer IV characteristics by recessing. It was originally thought that placing the p-gate on top would not allow control of the n-FET IV characteristics, and material control would be difficult. However, material control still was an issue with the back-gate an actually was more difficult.

The preferred method of fabricating the CFET would be to invert the structure and put the p-gate on top, as shown in Figure 4-1. This would reduce the area of the gate by orders of magnitude and also reduce the matching material control problem. This would help to confine the material control problem to a single layer, the n-layer.

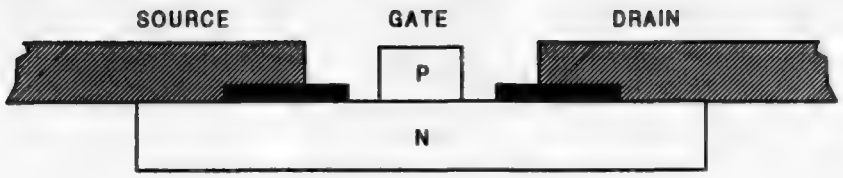


Figure 4-1. Inverted CFET

4.3.2 Co-Integration

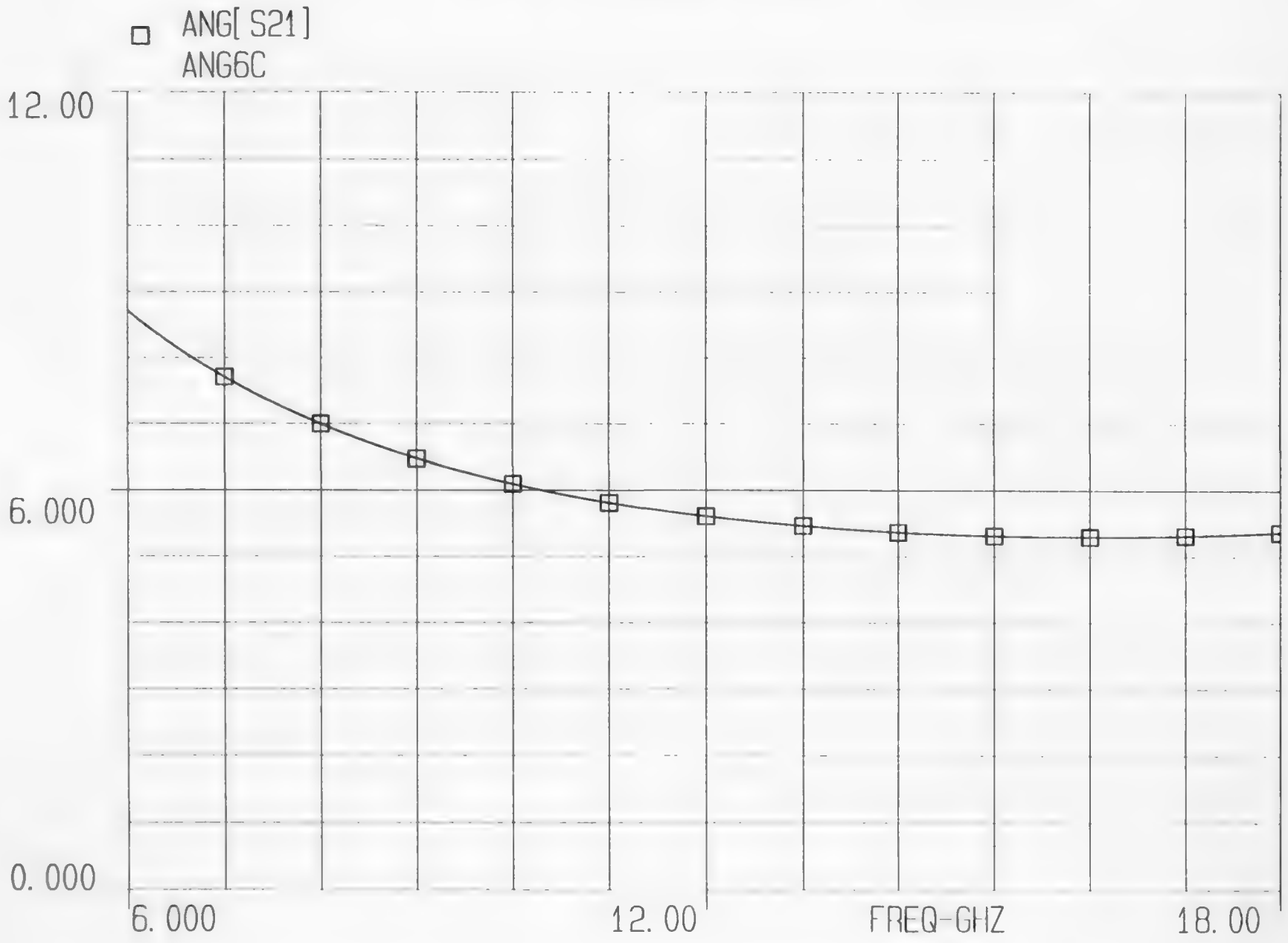
A technology thrust in the GaAs industry is co-integration of low noise amplifiers, power amplifiers, phase shifters, etc., onto a single chip. Ideally this would be achieved by a single technology (all MESFET or all PHEMT, for example). Multiple technologies would require similar type structures to achieve a practical process flow. The CFET structure is sufficiently different that it would be difficult to co-integrate with other monolithic devices. The performance of the CFET demonstrated on this program is not substantially better than present technologies to warrant as a stand-alone device technology, such as the vertical PIN (VPIN) diode.

4.3.3 Improved MESFETs

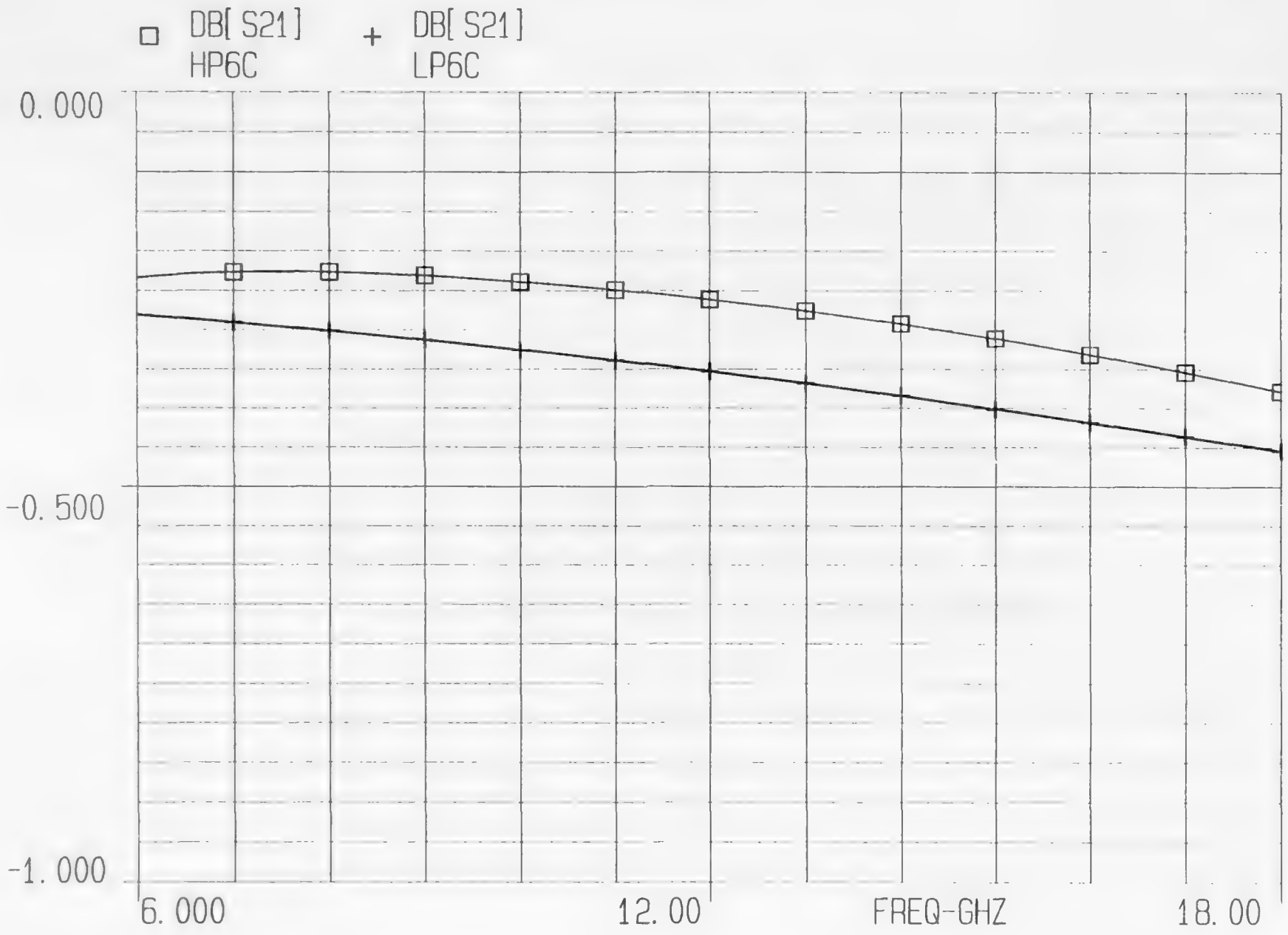
Recently TI has demonstrated MESFETs with improved figures of merit by reducing the source-drain spacing from 3.0 μm to 2.5 μm. This reduced the on-resistance with only a moderate increase in off-capacitance. This increased the figure of merit from 280 to 330 GHz. This structure is being used in some of the recently developed phase shifters with lower insertion loss. This was accomplished by modifying the pilot line design rules and more careful monitoring of the source-drain metallization process. This has been accomplished with very little effect on device yield.

APPENDIX A

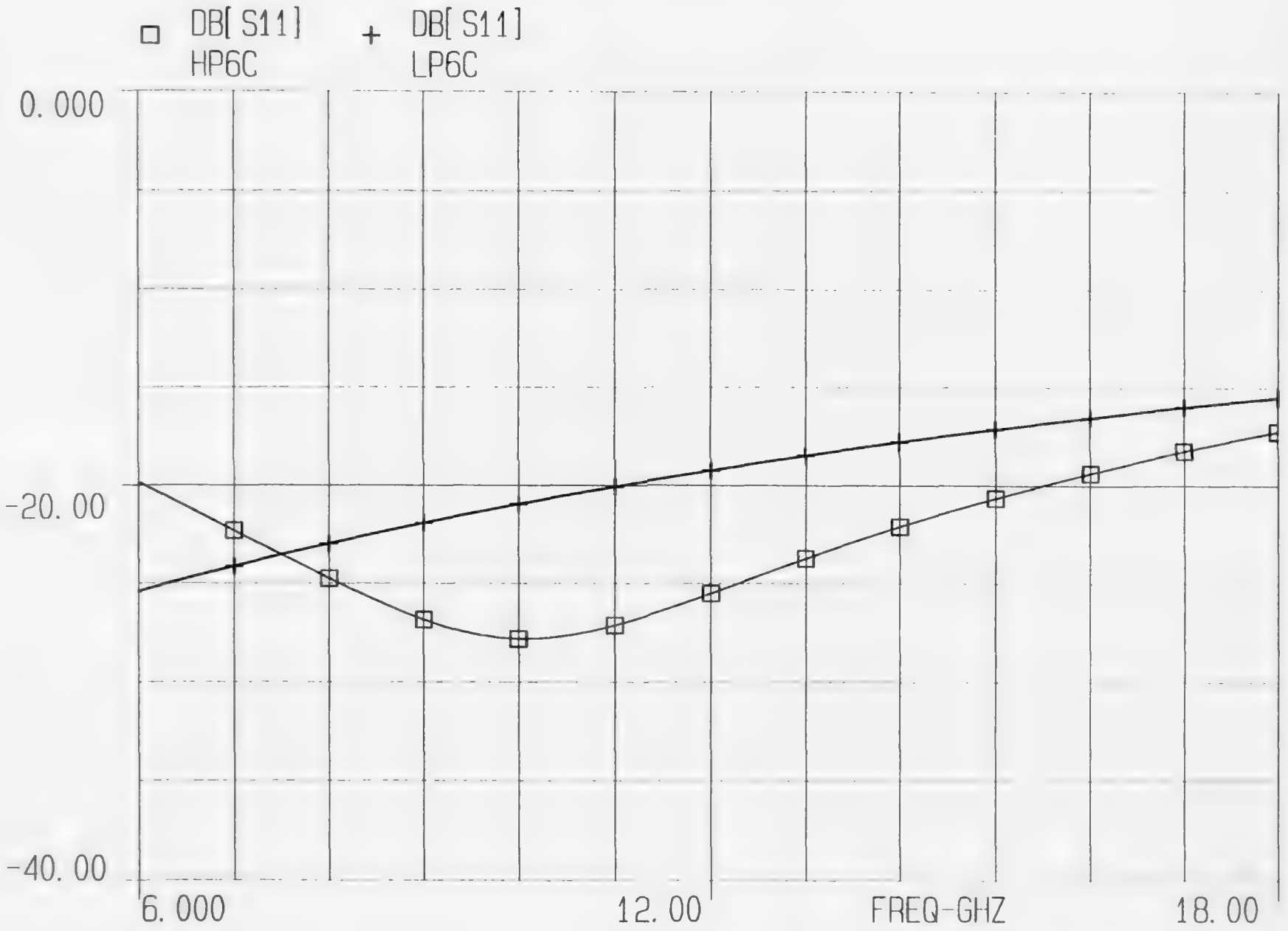
5.625° BIT PHASE SHIFT



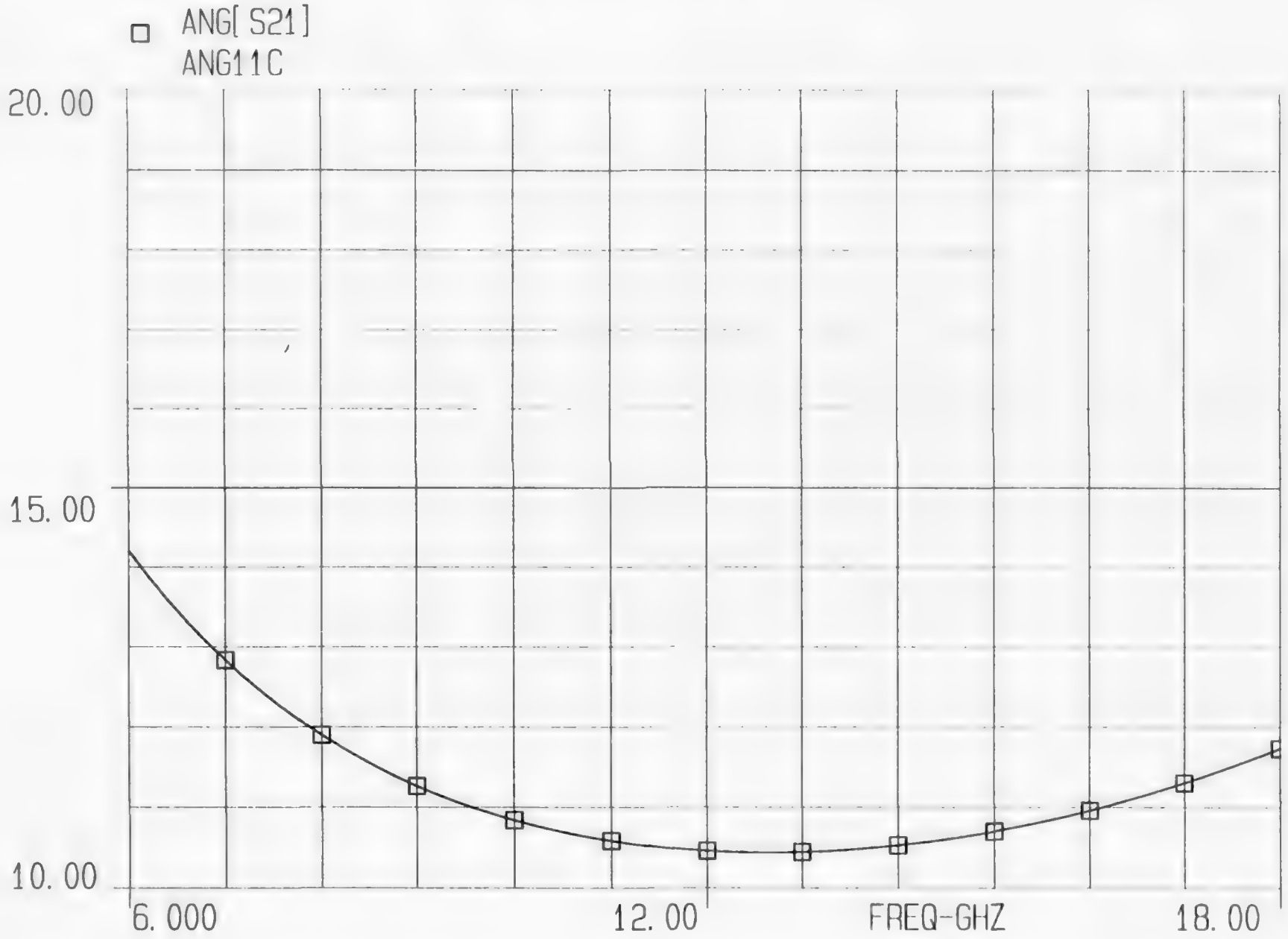
5.625° BIT INSERTION LOSS



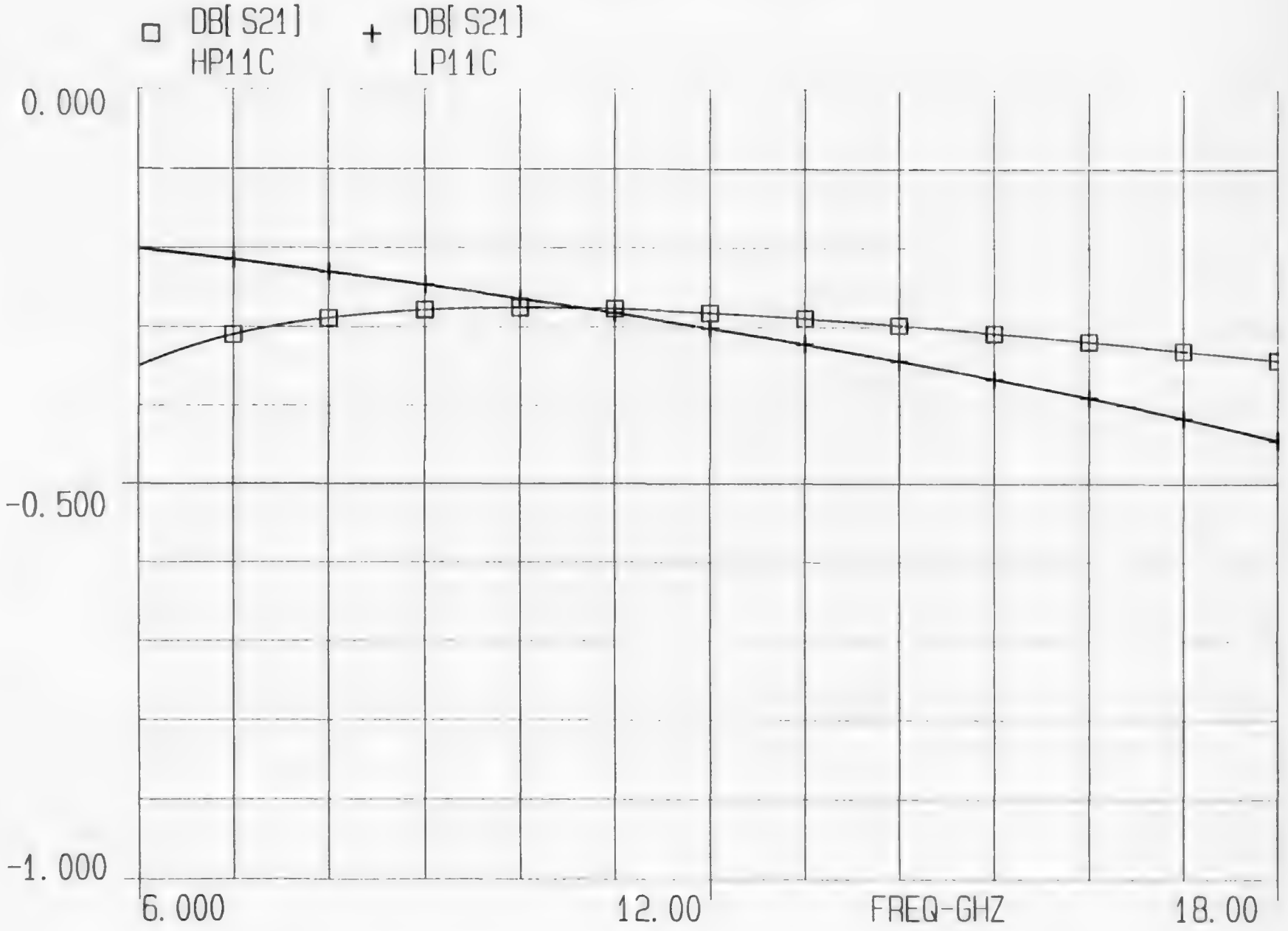
5.625° BIT RETURN LOSS



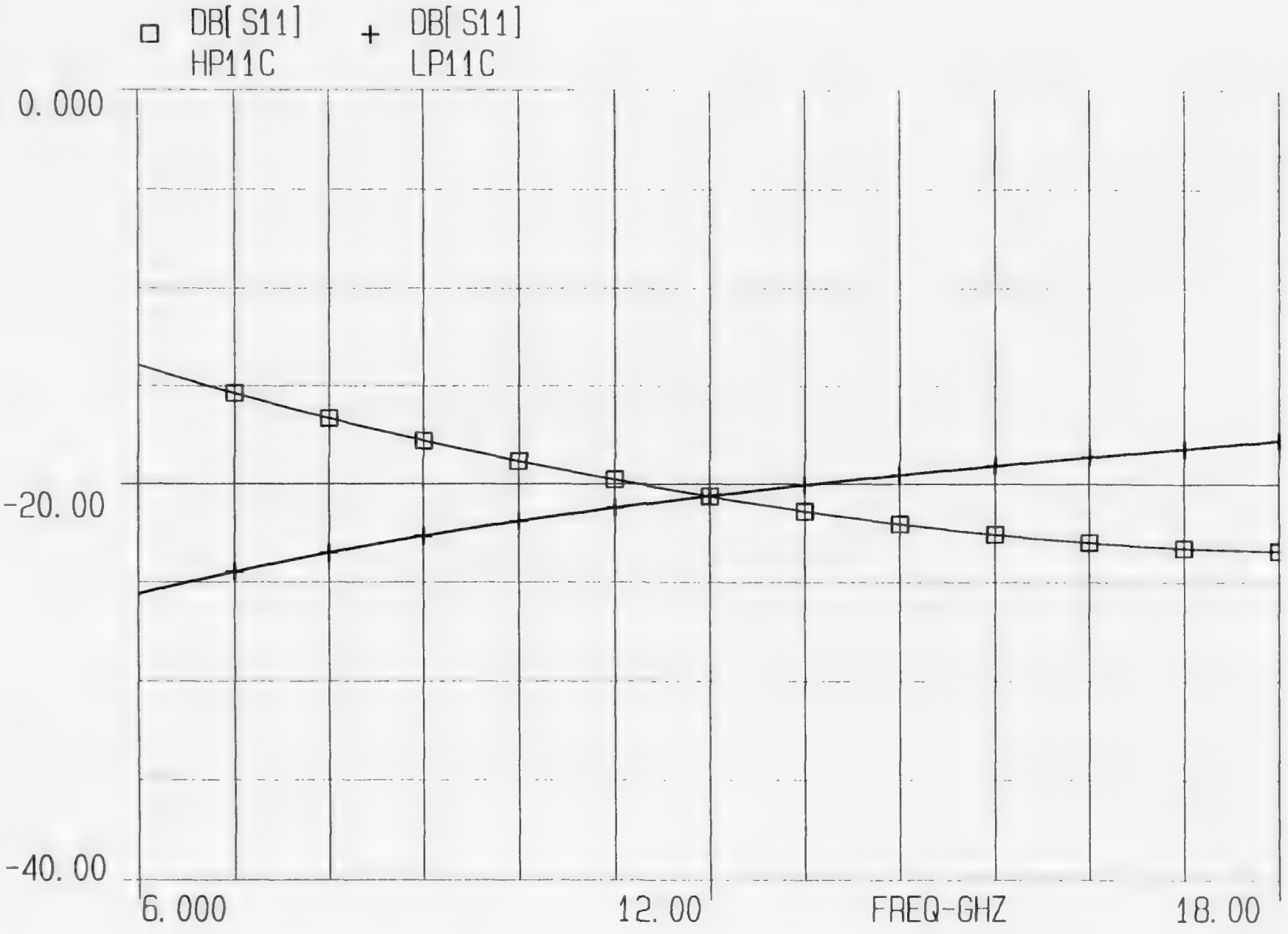
11.25° BIT PHASE SHIFT



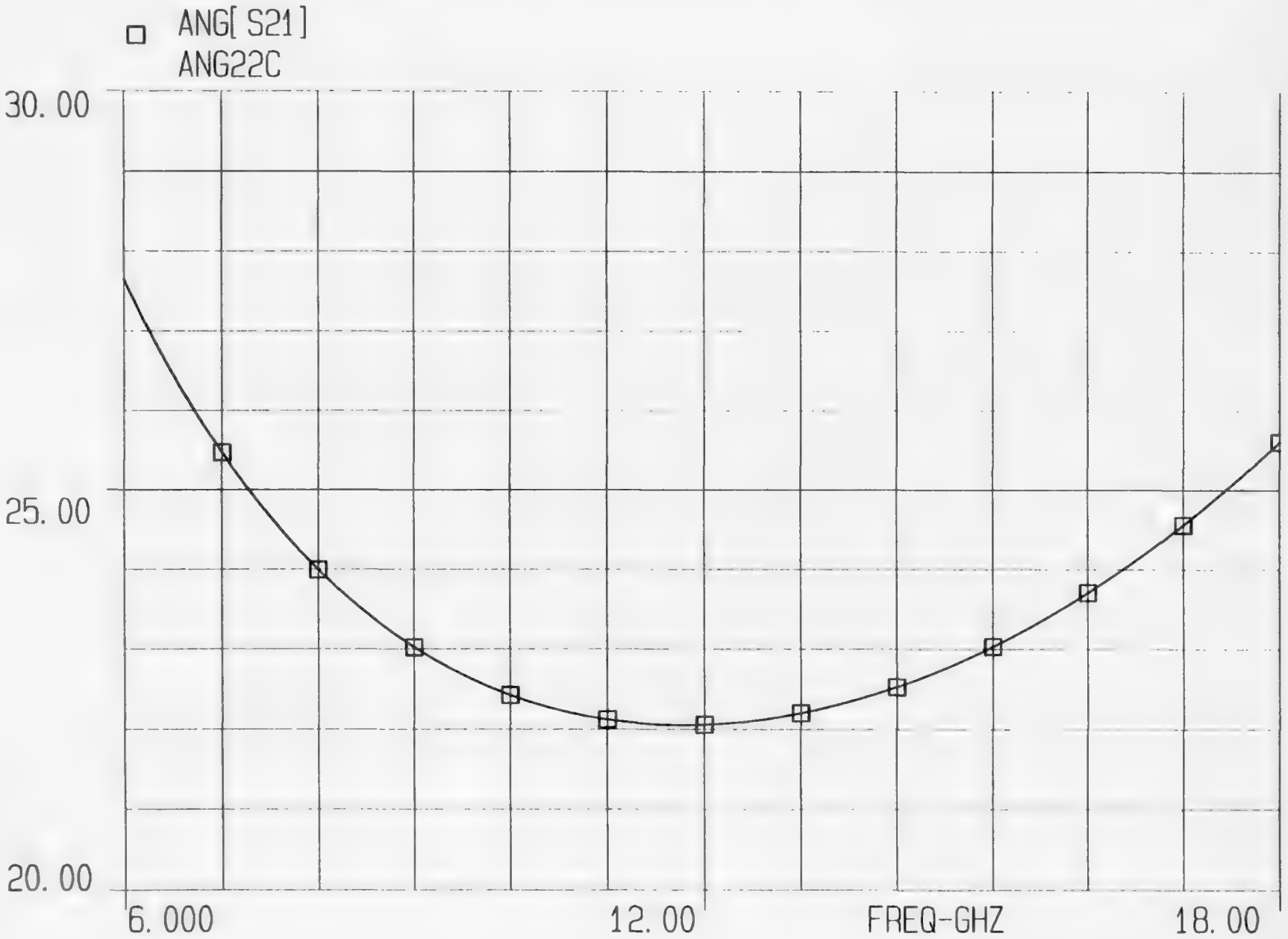
11.25° BIT INSERTION LOSS



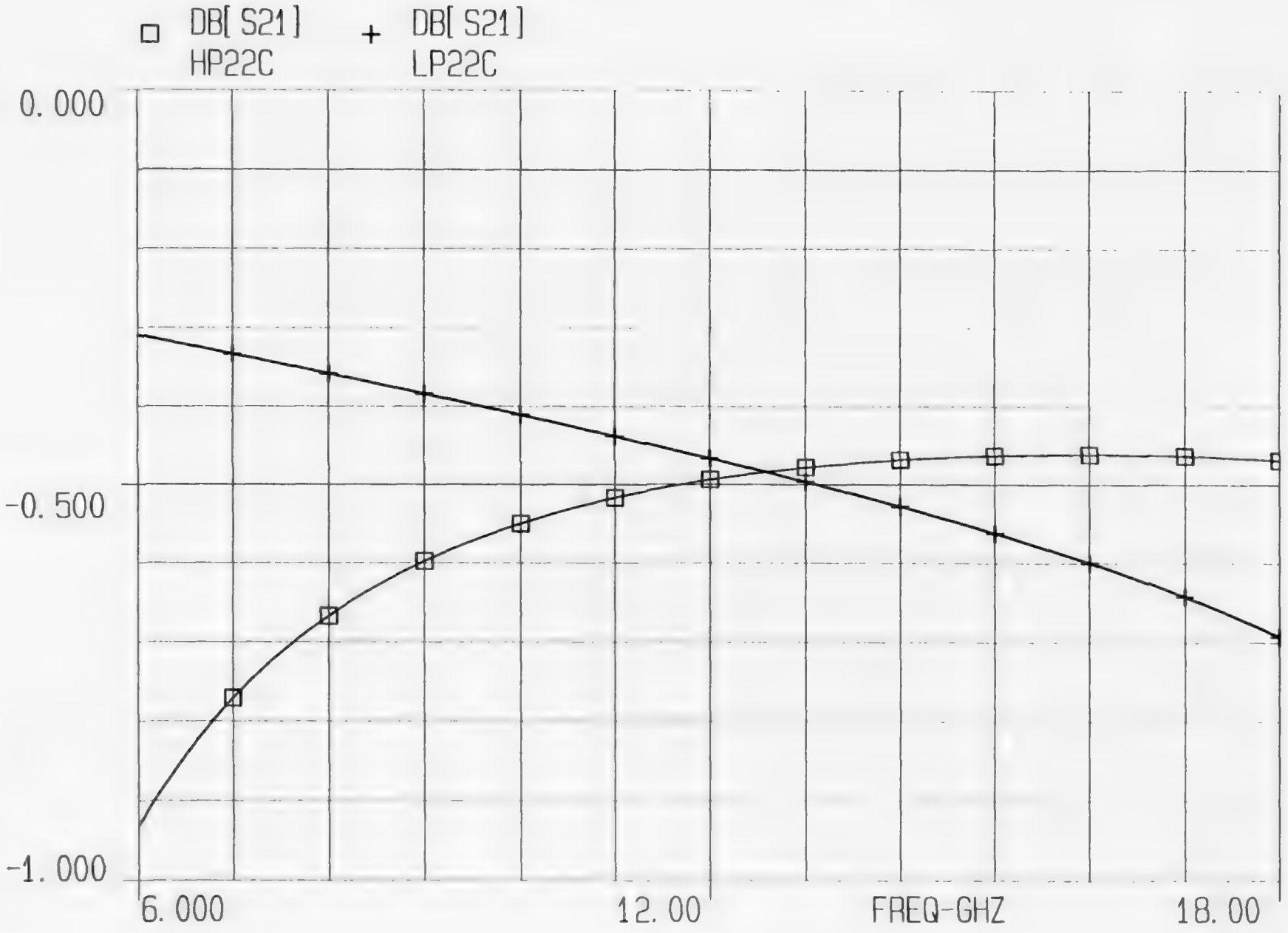
11.25° BIT RETURN LOSS



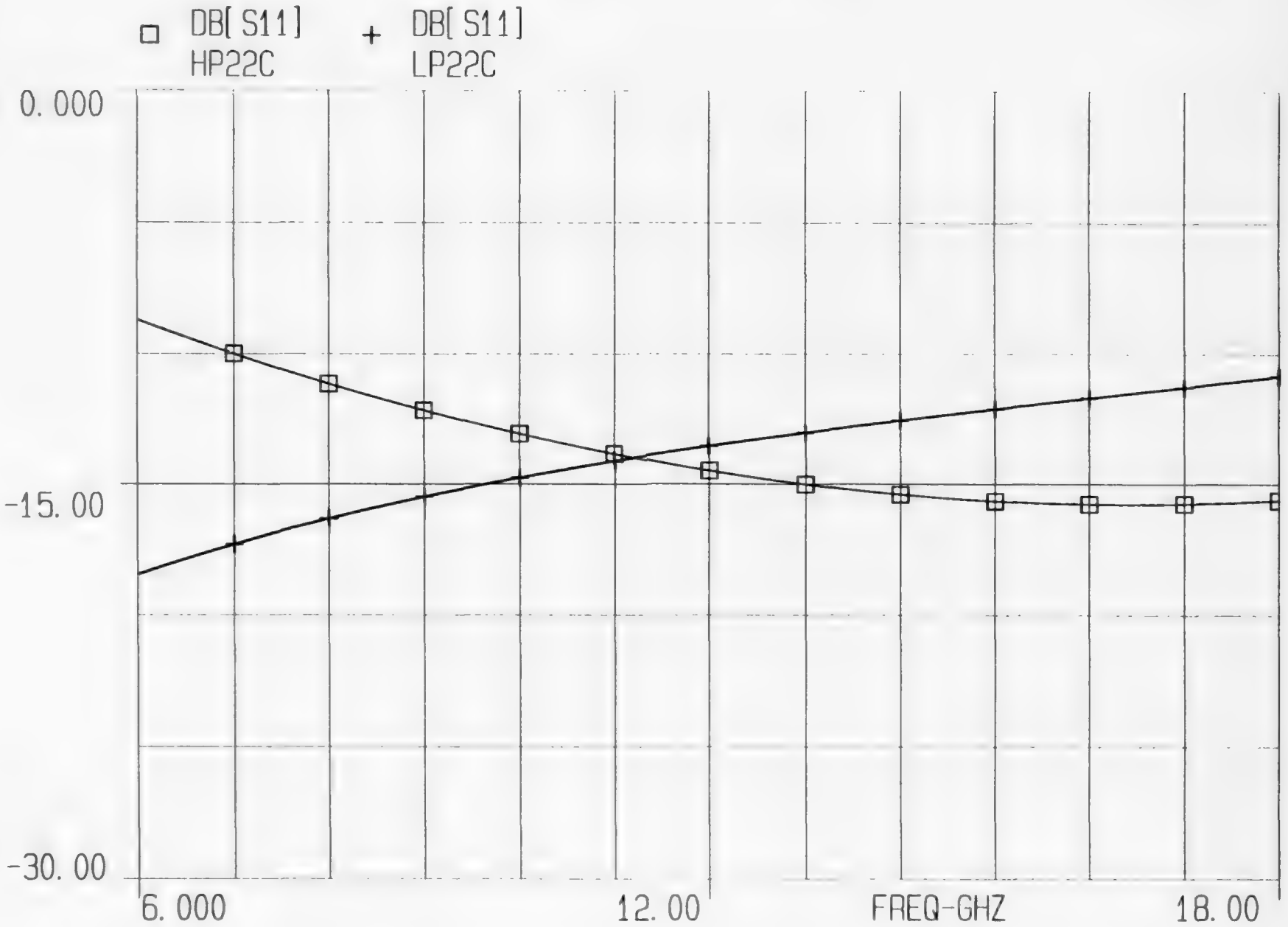
22.5° BIT PHASE SHIFT



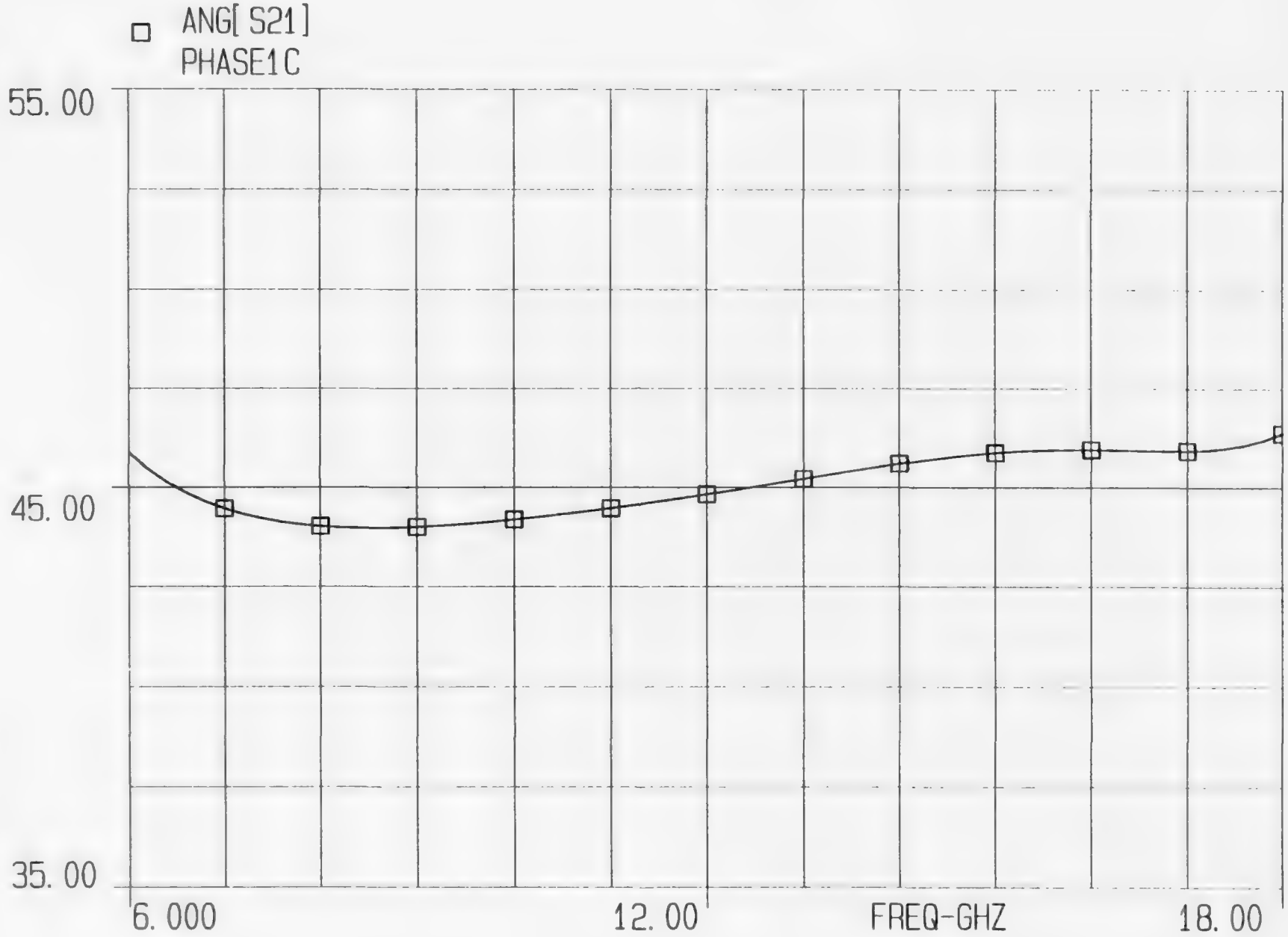
22.5° BIT INSERTION LOSS



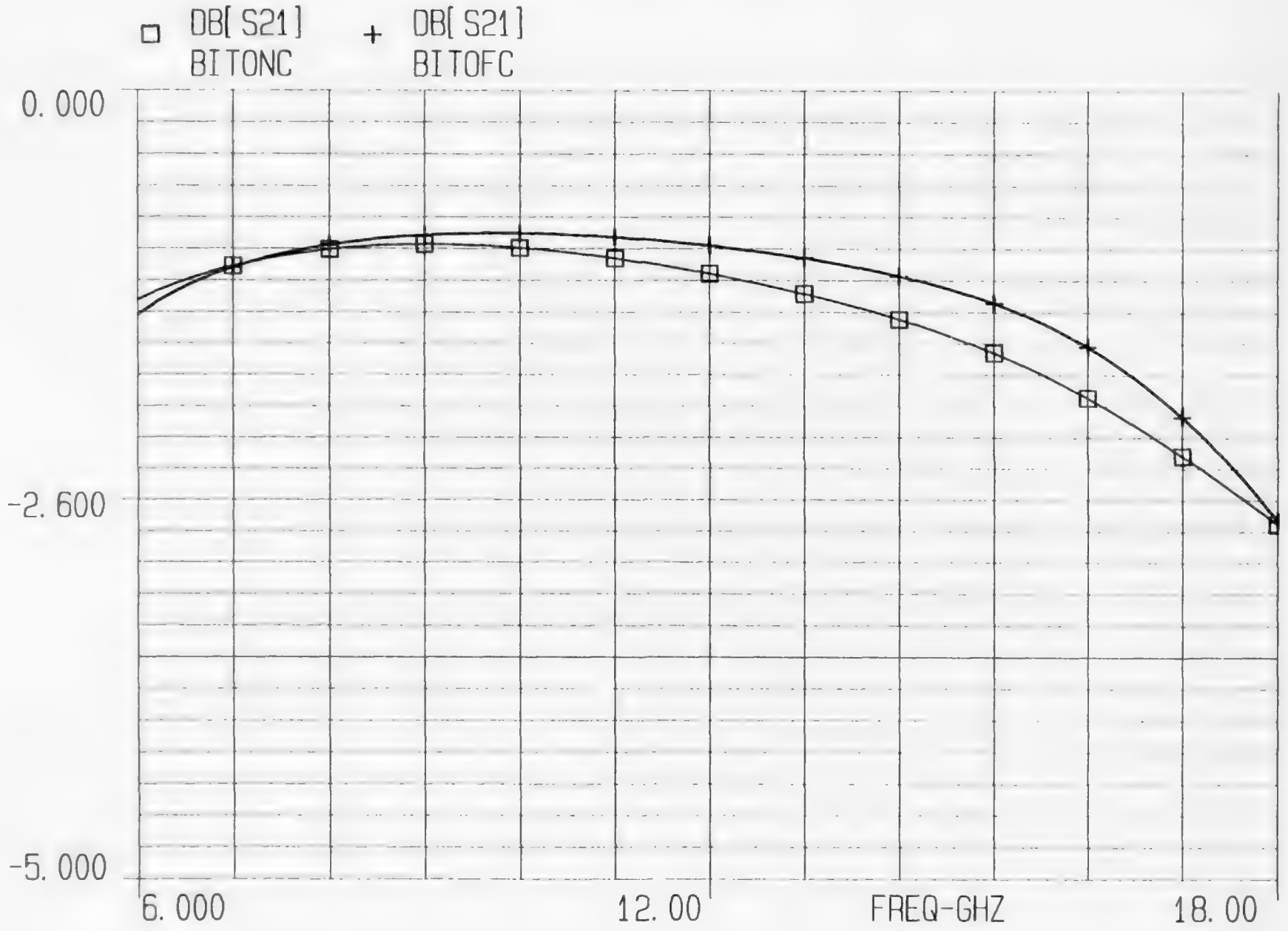
22.5° BIT RETURN LOSS



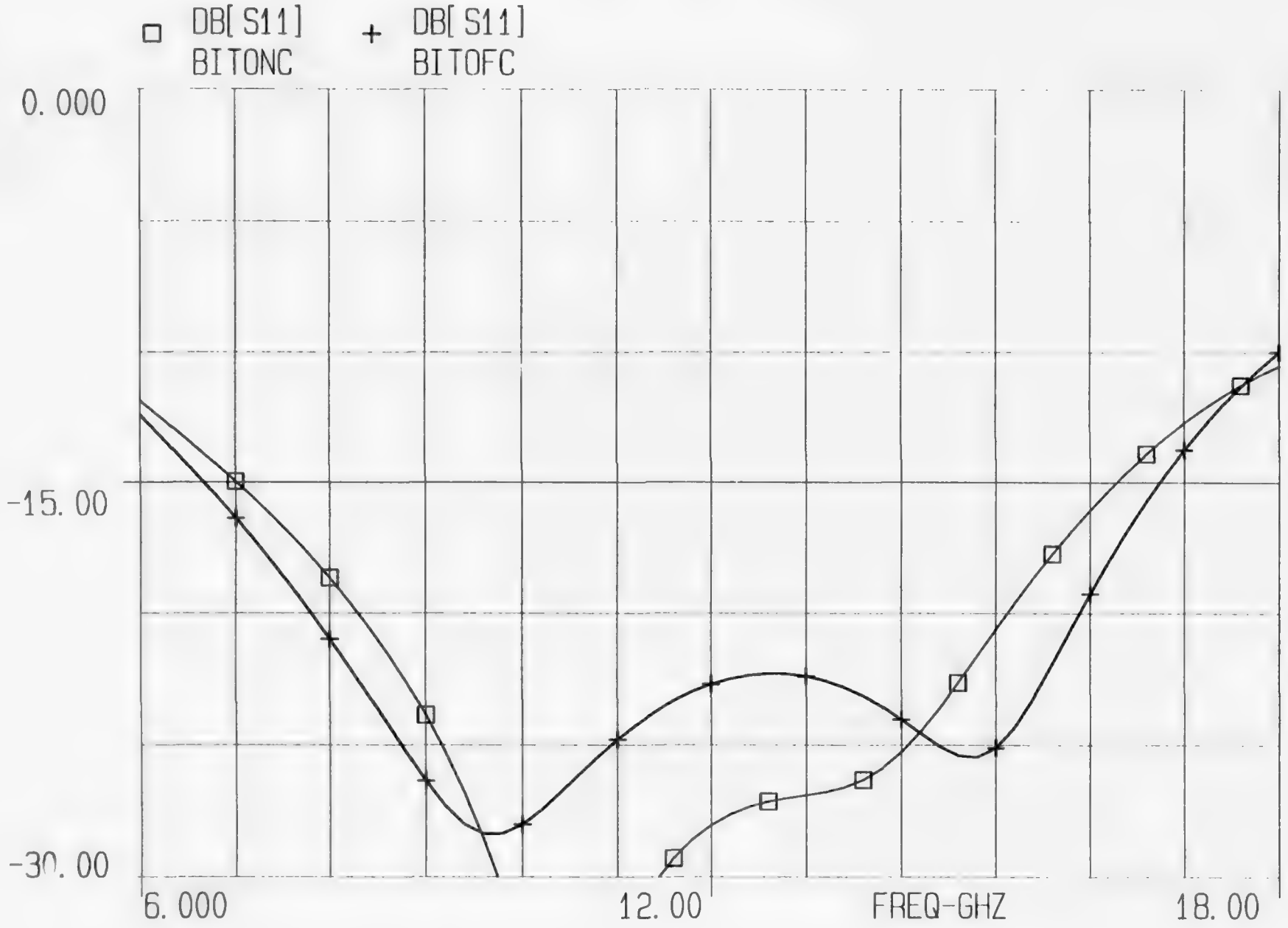
45° BIT PHASE SHIFT



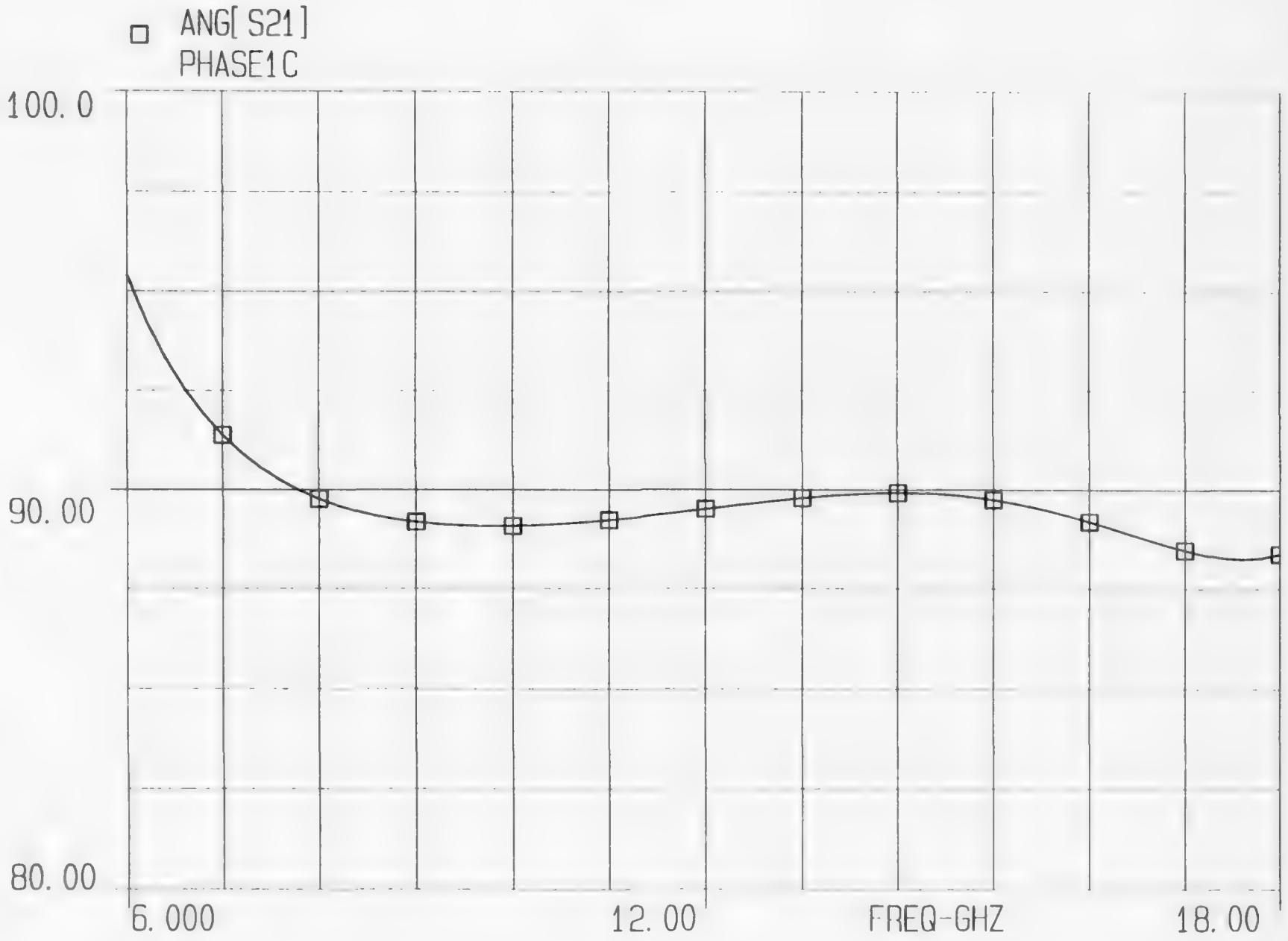
45° BIT INSERTION LOSS



45° BIT RETURN LOSS

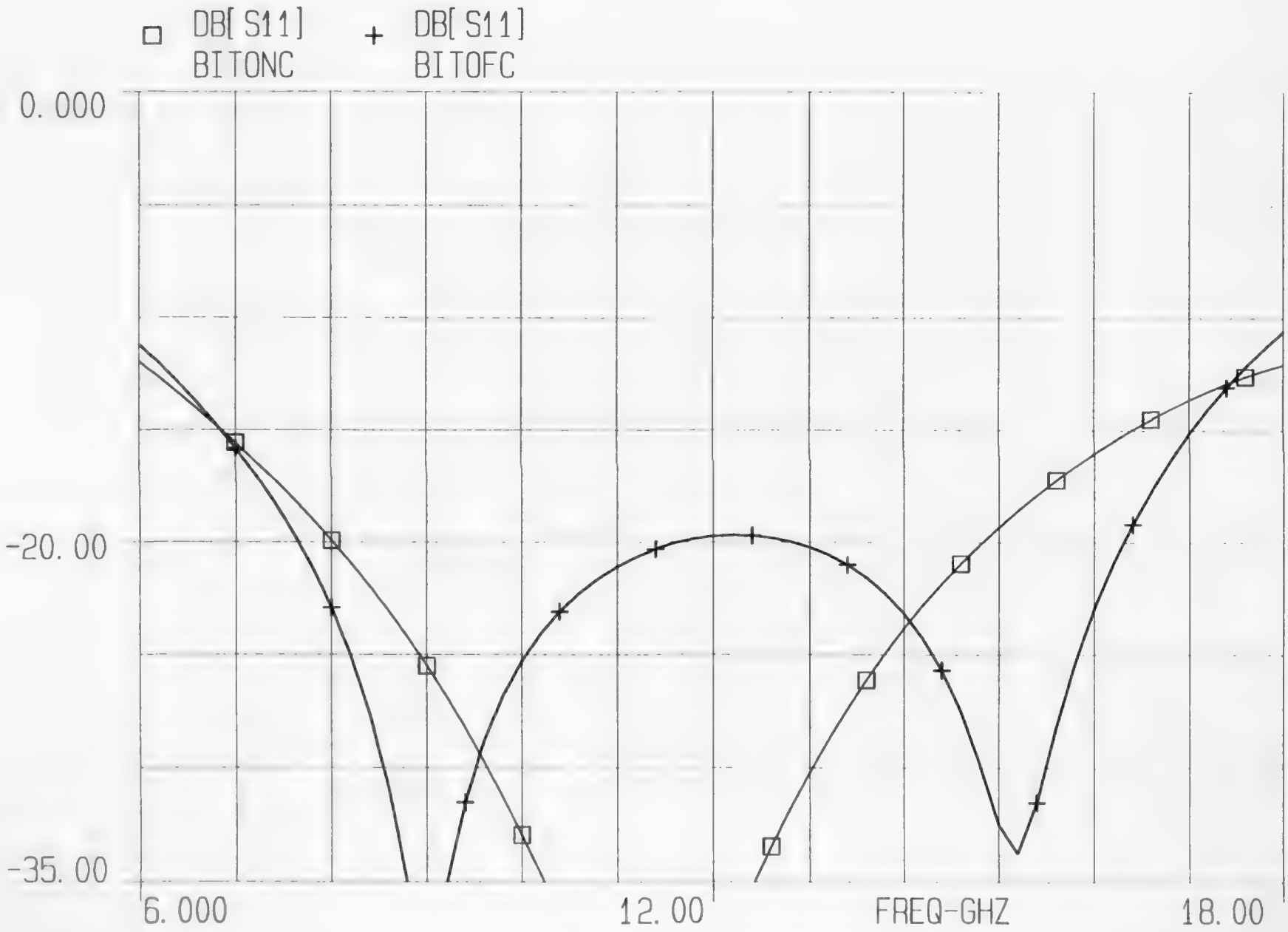


90° BIT PHASE SHIFT

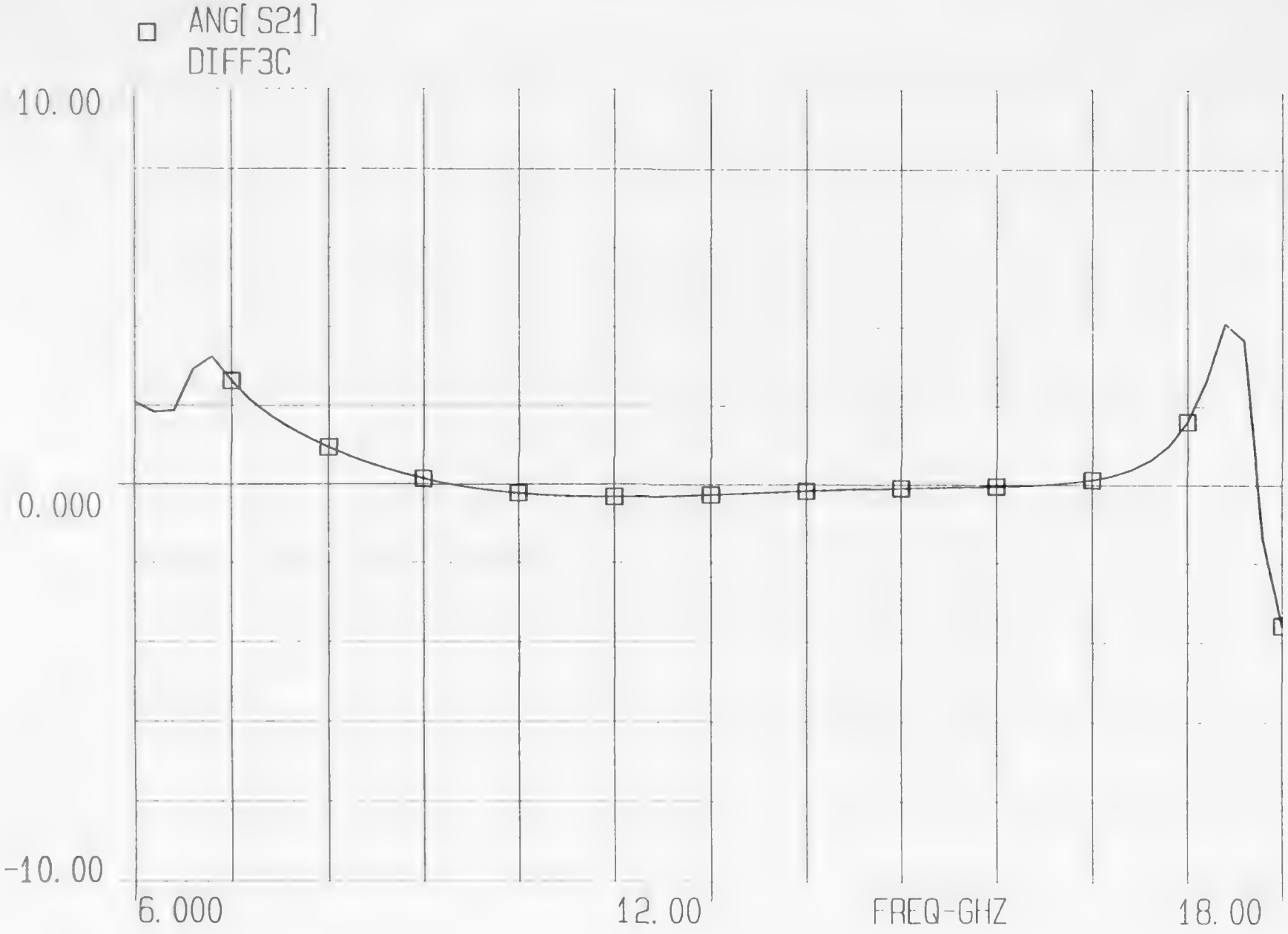


90° BIT INSERTION LOSS

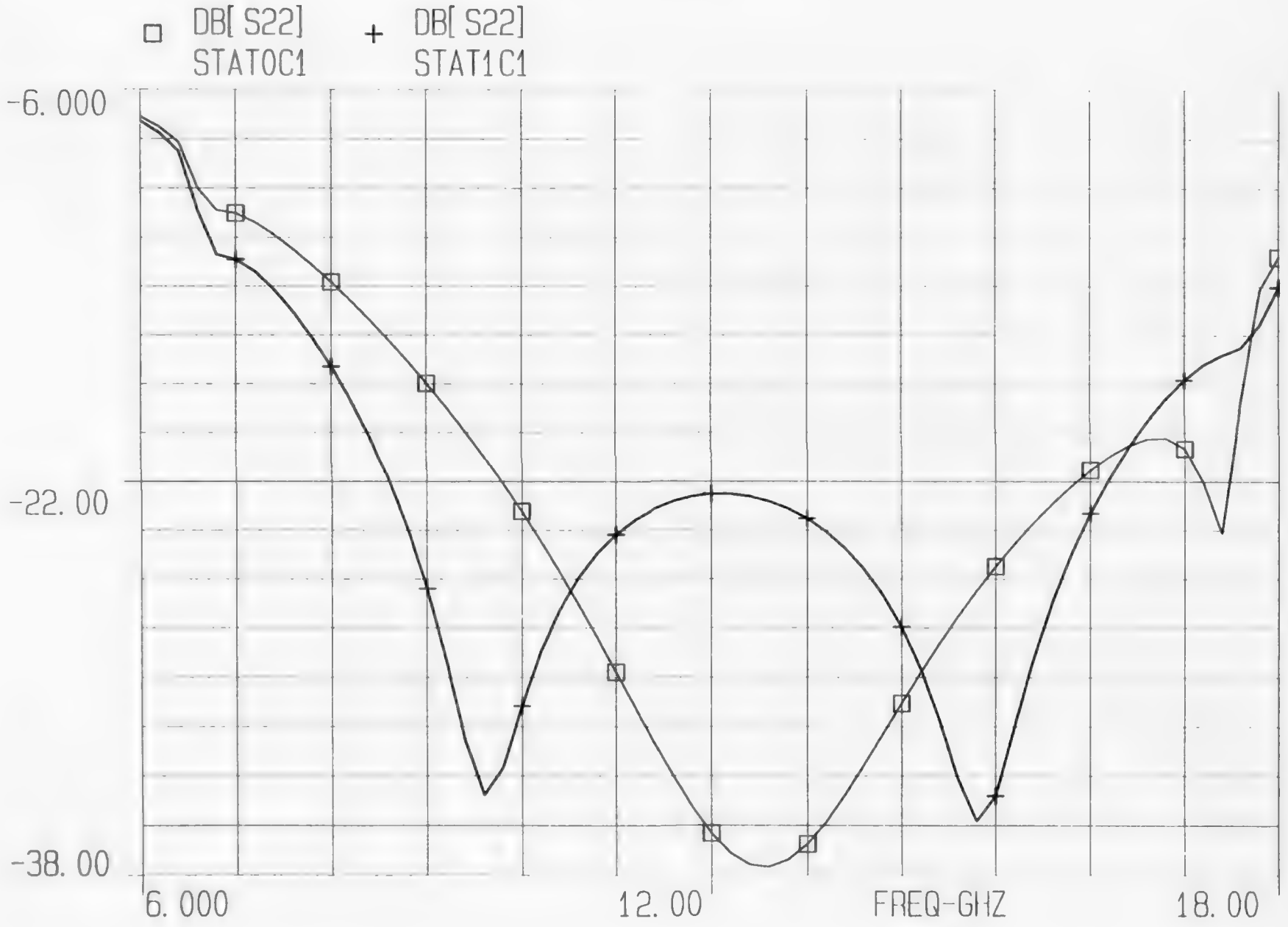
90° BIT RETURN LOSS



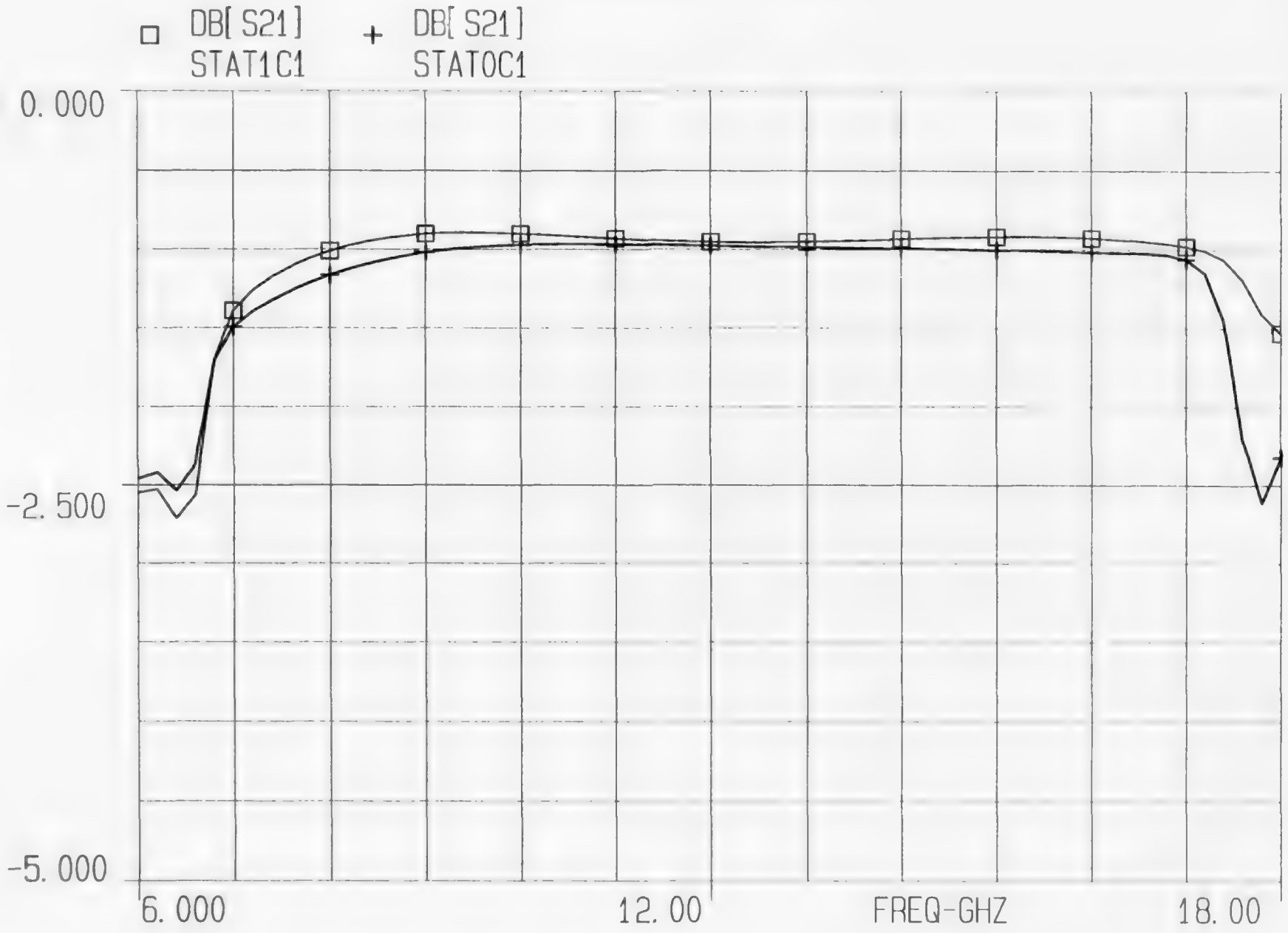
180° BIT PHASE ERROR



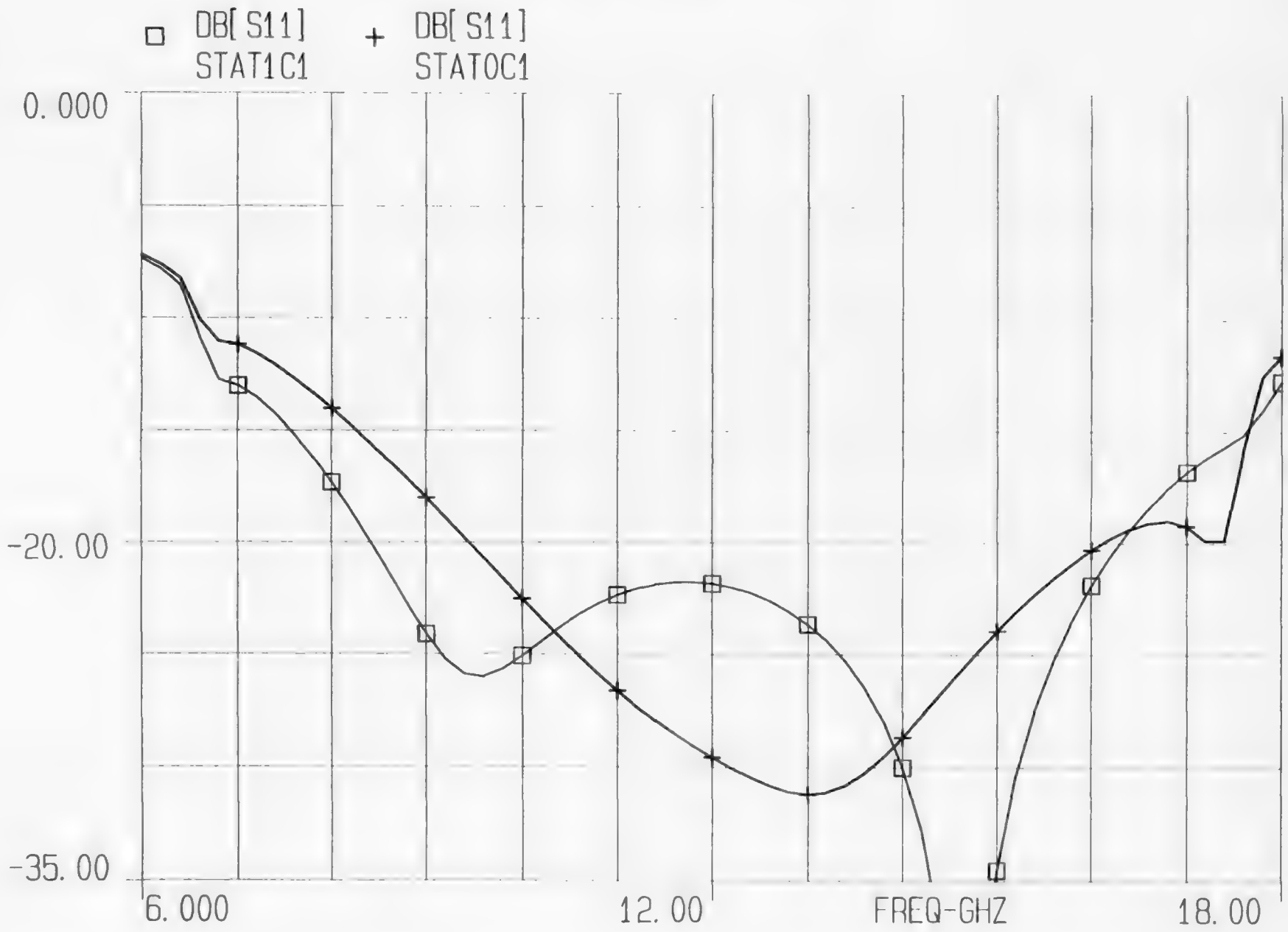
180° BIT PHASE SHIFT

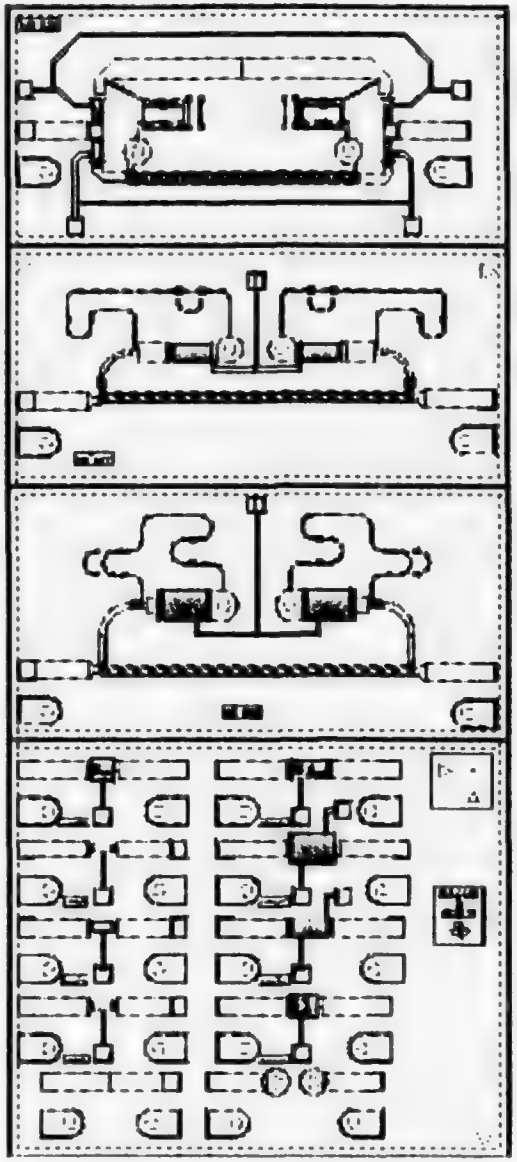


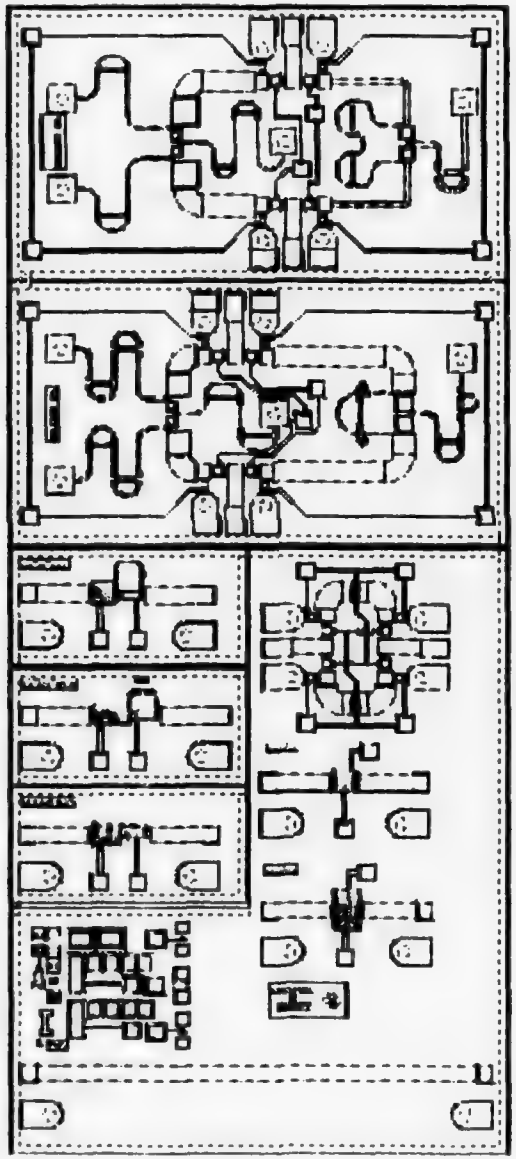
180° BIT INSERTION LOSS



180° BIT RETURN LOSS

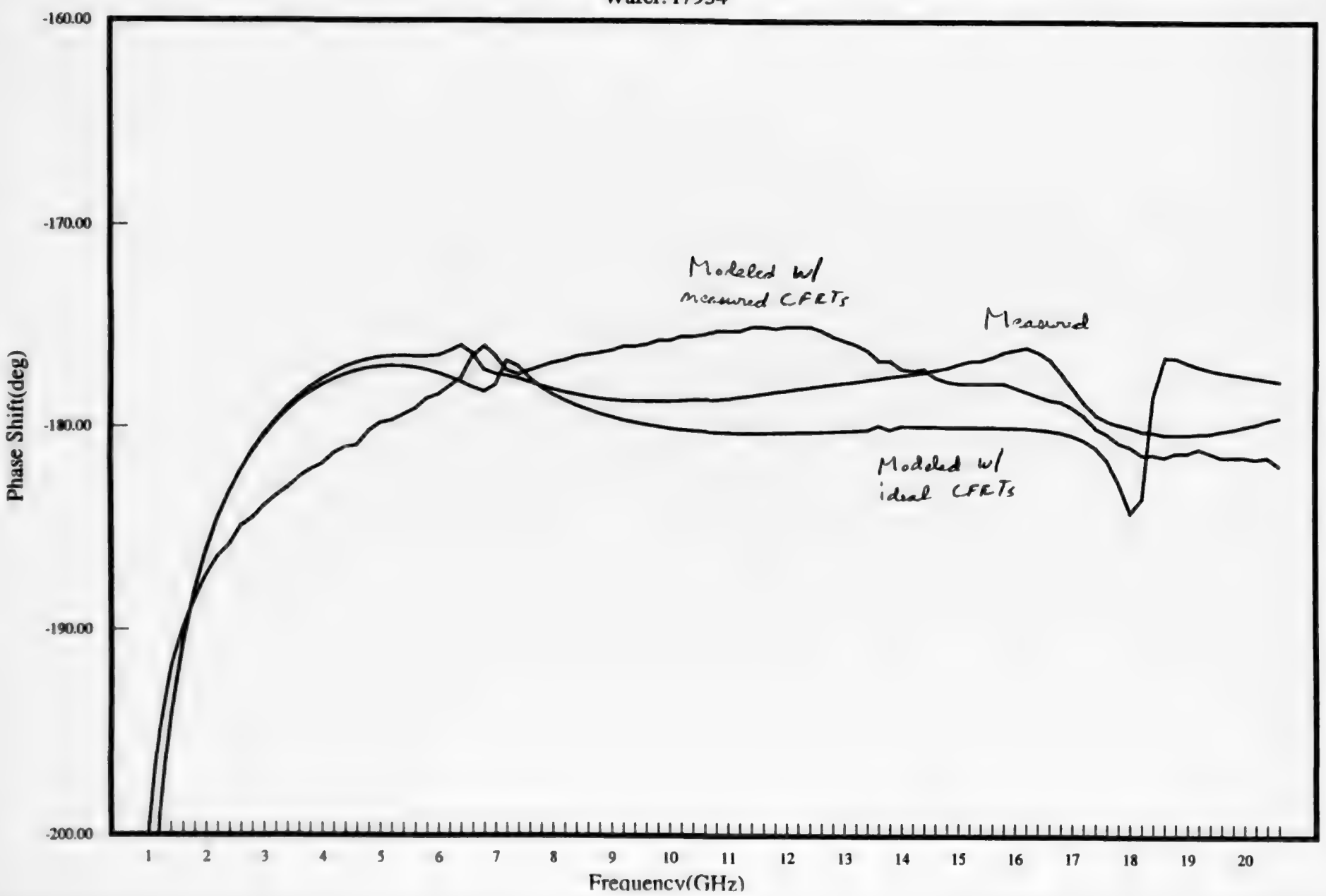



180° BIT
90° BIT
45° BIT
CFET TEST STRUCTURES
CALIBRATION STRUCTURE

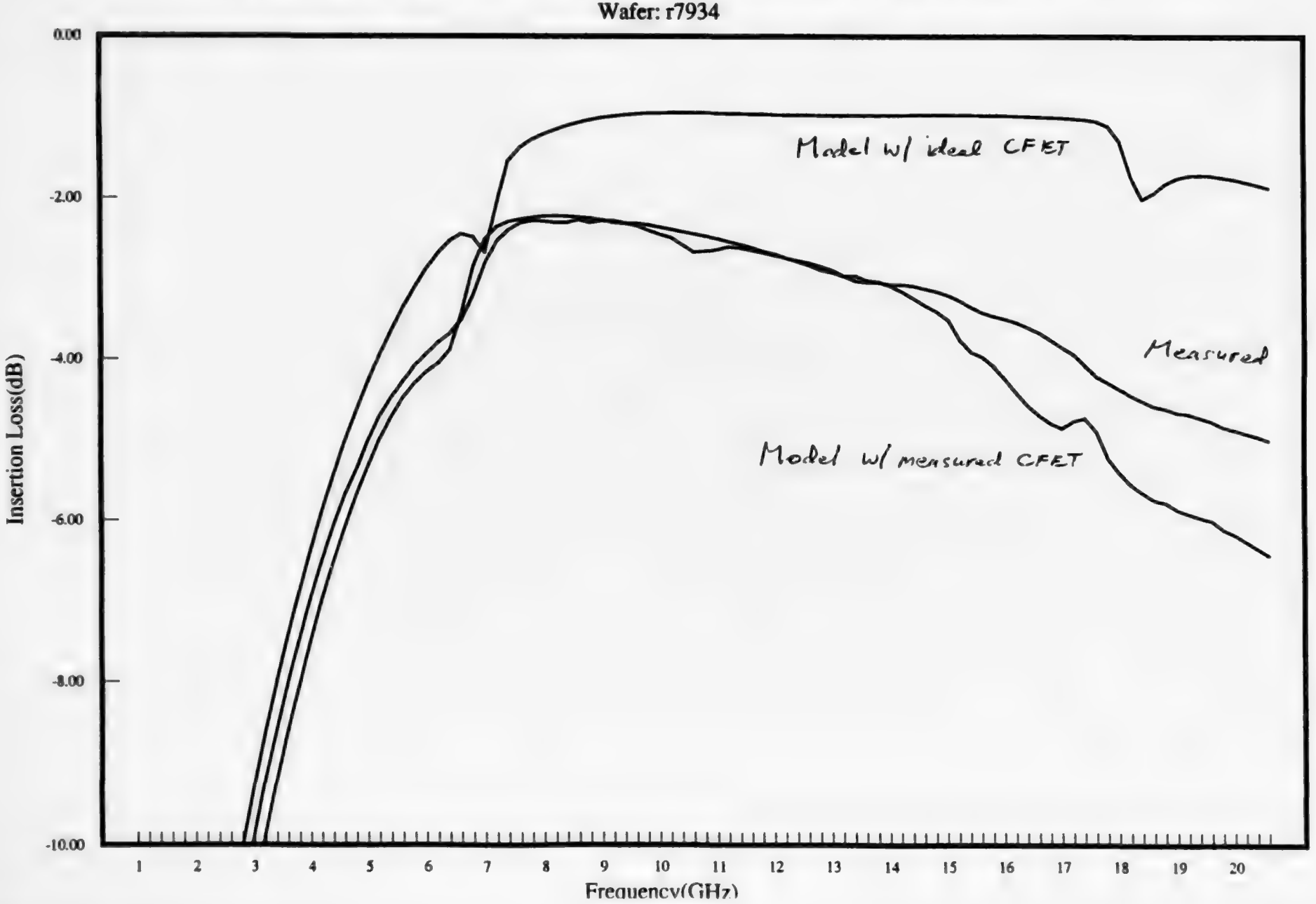

90° ALLPASS/HIGHPASS
45° ALLPASS/HIGHPASS
22.5° BIT
11.25° BIT
5.625° BIT
SPDT
CFET TEST STRUCTURES
PROCESS TEST CELL
DELAY LINE

APPENDIX B

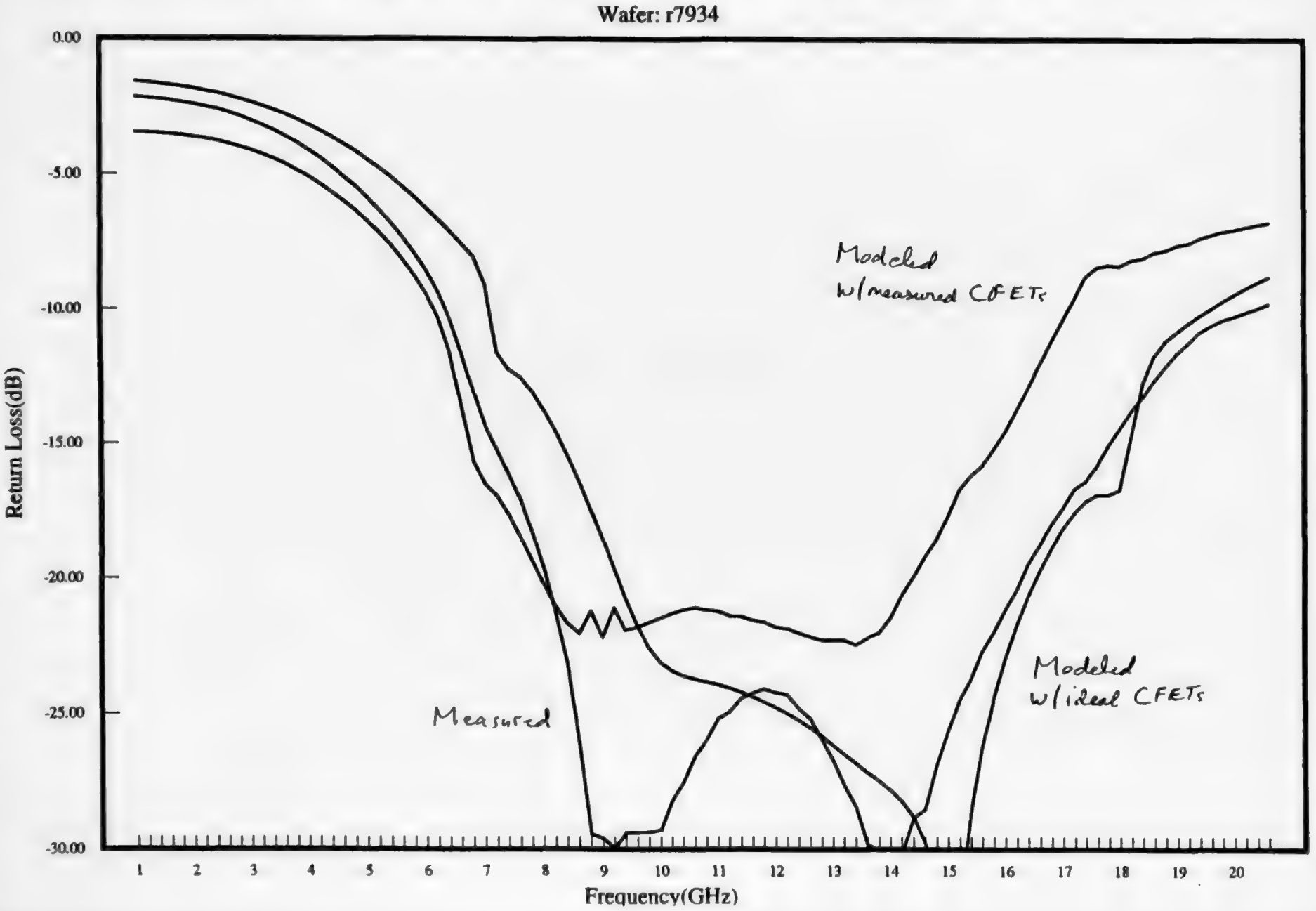
180 DEG PHASE SHIFTER



180 DEG PHASE SHIFTER

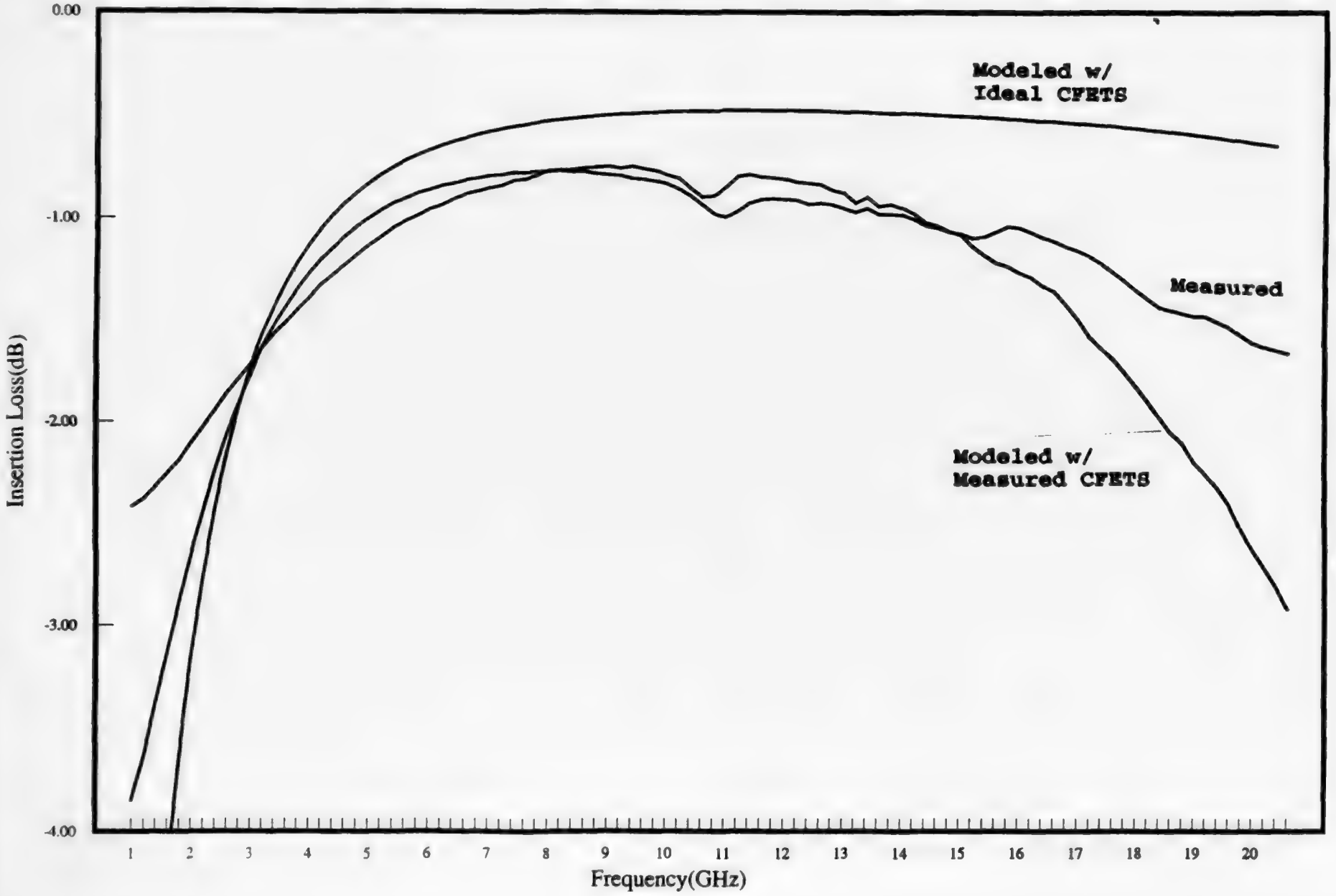


180 DEG PHASE SHIFTER

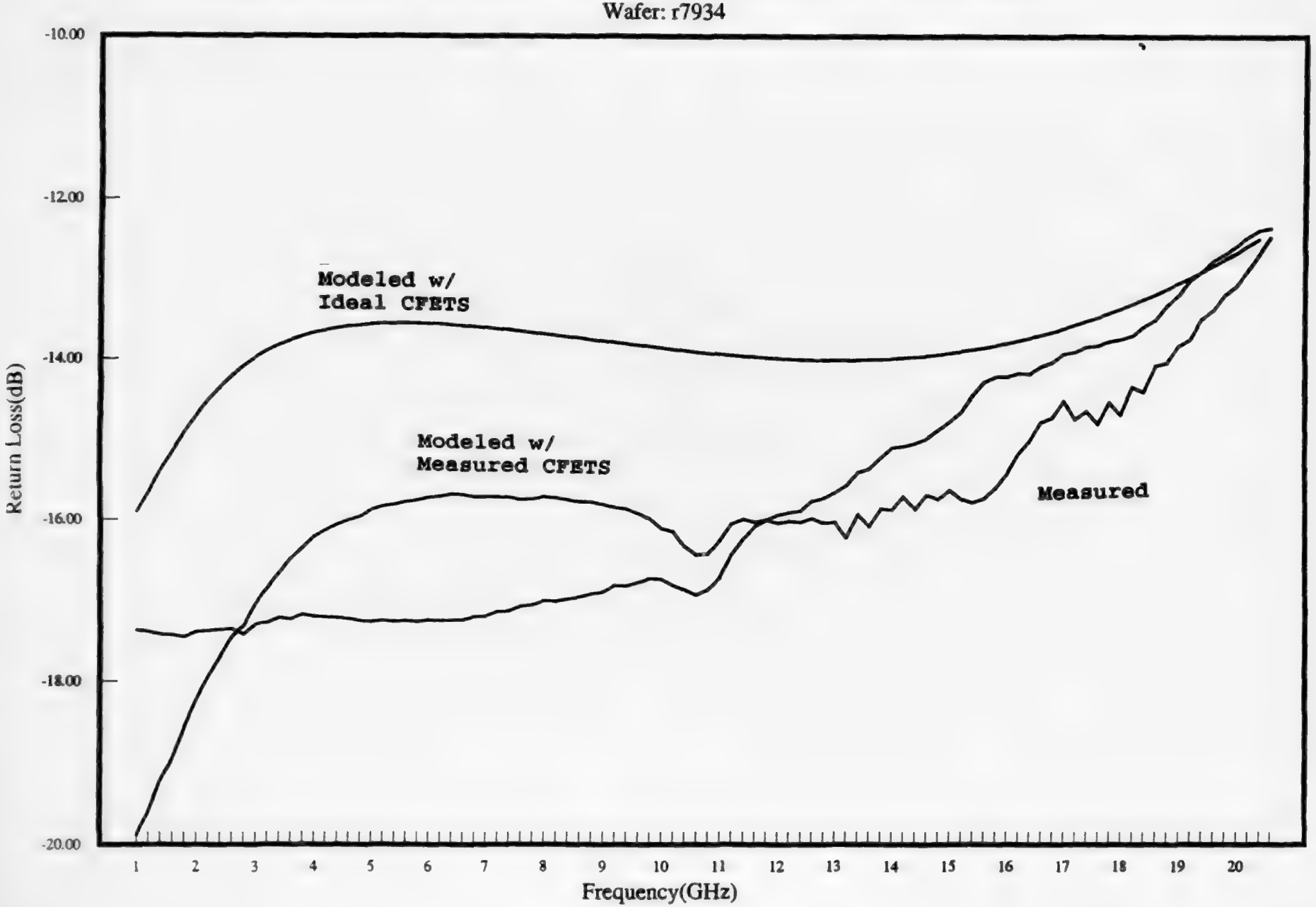


22.5 DEG PHASE SHIFTER

Wafer: r7934



22.5 DEG PHASE SHIFTER



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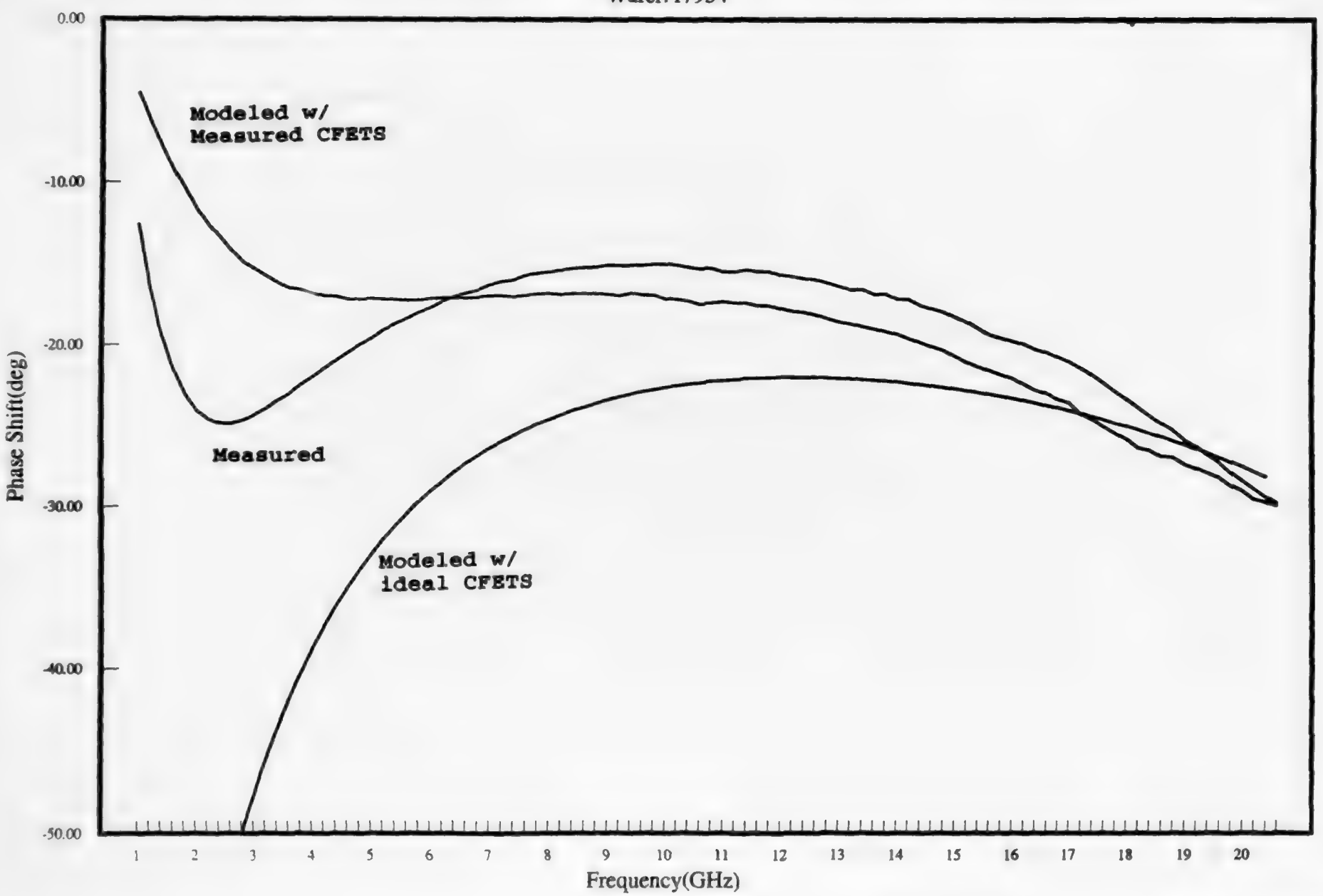
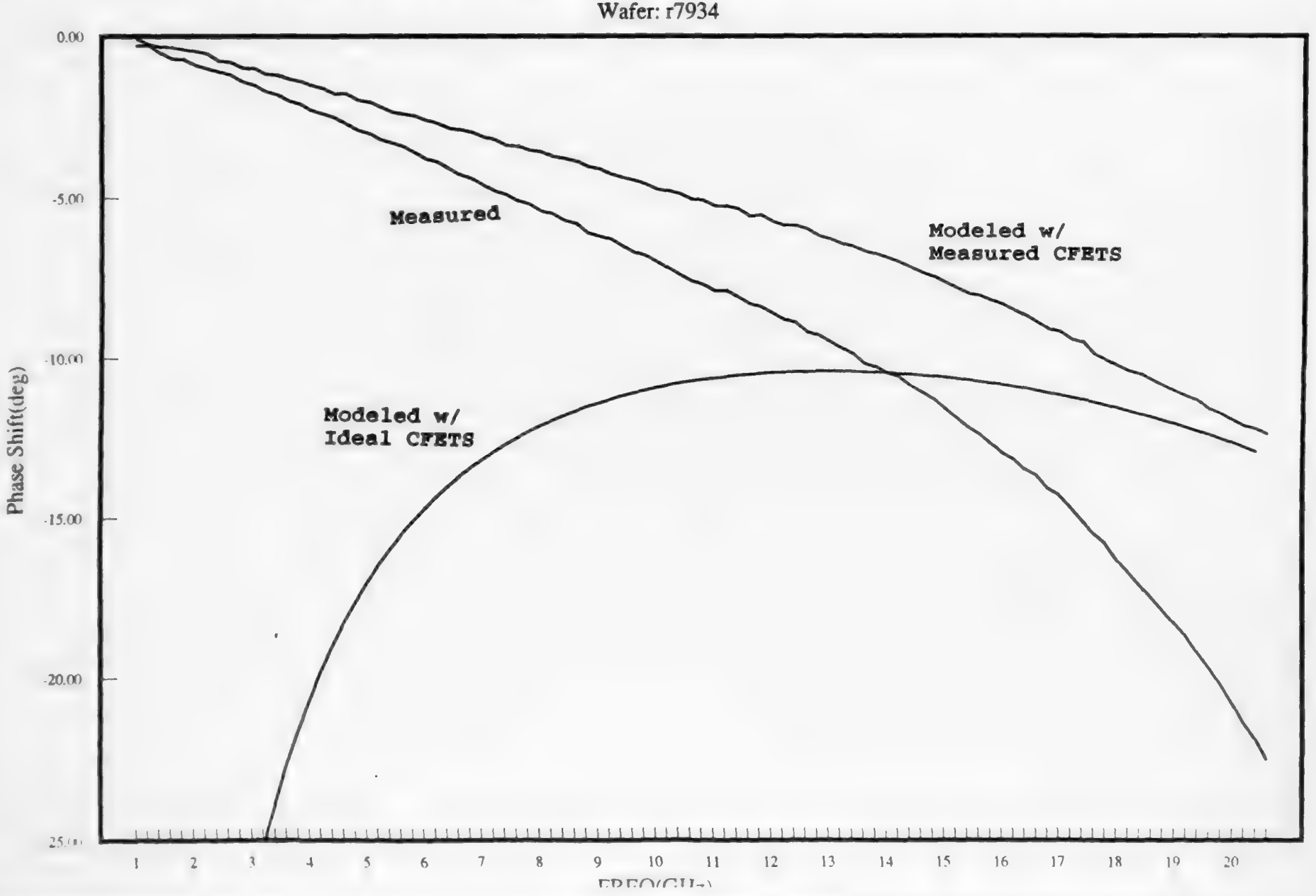
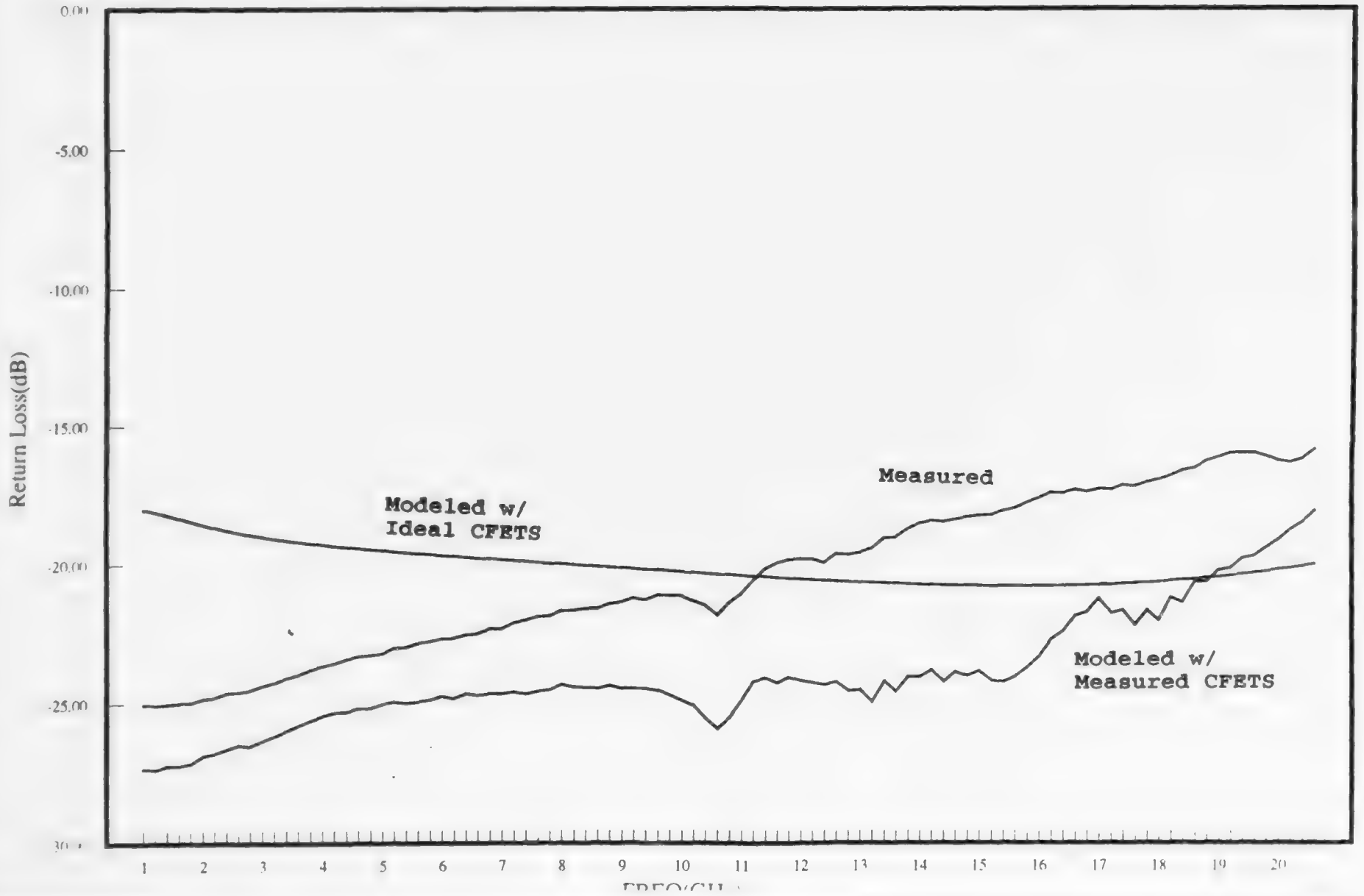


11.25 DEG PHASE SHIFTER



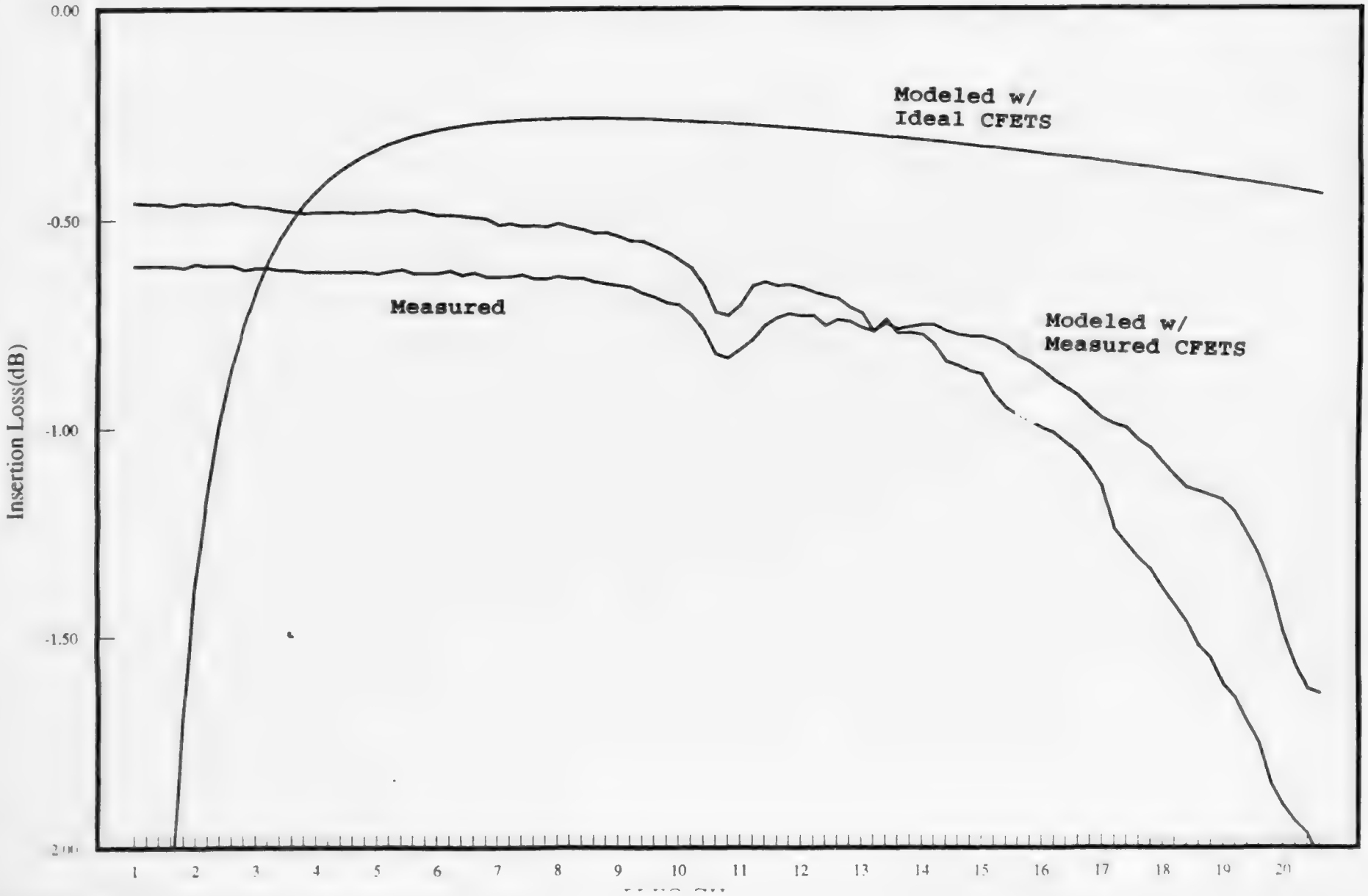
11.25 DEG PHASE SHIFTER

Wafer: r7934



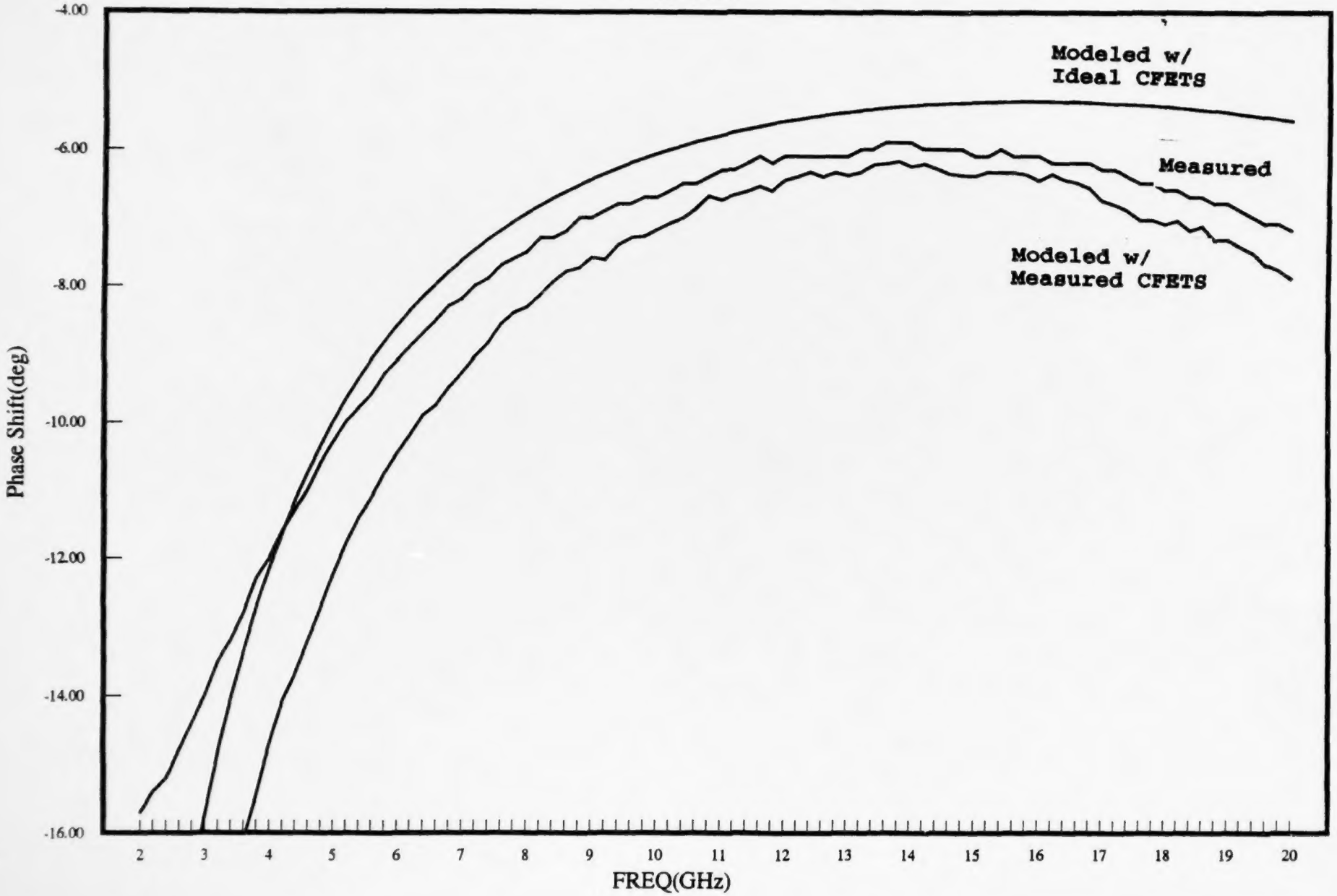
11.25 BIT PHASE SHIFTER

Wafer: r7934

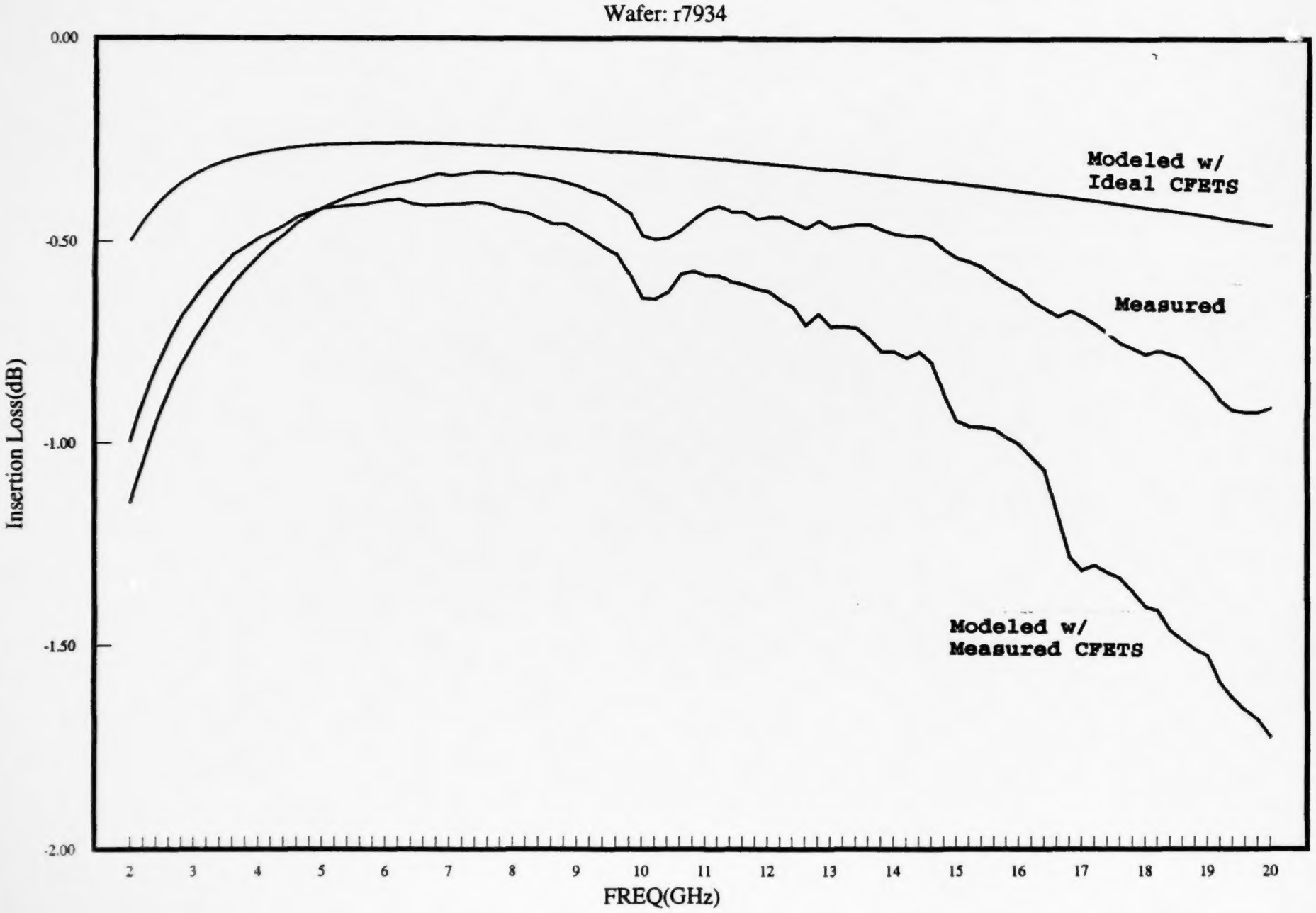


5.6 DEG PHASE SHIFTER

Wafer: r7934



5.6 DEG PHASE SHIFTER



5.6 DEG PHASE SHIFTER

Wafer: r7934